Development of Quartz MEMS Microfabrication Technologies and Their Application to Capacitive Tilt Sensors

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Contents

Figures

Tables

Chapter 1 Introduction

1.1 MEMS

Microelectromechanical systems (MEMS) have recently become an important area of technology, building on the success of the microelectronics industry over the past 50 years. MEMS combine mechanical and electrical function in devices at very small scales. Examples include pressure sensors, accelerometers, gyroscopes and optical devices, as well as chemical, biomedical and fluidic applications [1].

MEMS are the integration of mechanical elements, sensors, actuators, and electronics on a common silicon substrate through microfabrication technology. MEMS devices attracted more and more attention for its charming characteristics, such as miniaturization, multiplicity and microelectronics and so on [2]. The success of MEMS as a key technology in the twenty first century depends in no small part on the solution of materials issues associated with the design and fabrication of complex MEMS devices [1].

1.1.1. MEMS fabrication process

Several fabrication processes account for the vast majority of MEMS devices. These are surface micromachining, bulk micromachining and molding processes and so on.

Surface micromachining [3] has evolved directly from the CMOS (complementary metal-oxide-semi-conductor) processes used to fabricate VLSI (very large scale integration) devices. These devices consist of thin deposited layers of conductors, insulators, and semiconductors and passivation layers on doped silicon wafer substrates. In VLSI devices the layers are deposited, patterned and etched to yield highly integrated electronic devices with very small feature sizes. In surface micromachined MEMS the layers are patterned and etched to yield electromechanical elements or are used as sacrificial layers to allow motion of the mechanical layers [1]. Advantages of surface

micromachining are a) structural and spacer features, especially thicknesses, can be smaller than 10 pm in size, b) the micromachined device footprint can often be much smaller than bulk wet-etched devices, c) it is easier to integrate electronics below surface microstructures, and d) surface microstructures generally have superior tolerance compared to bulk wet-etched devices. The primary disadvantage is the fragility of surface microstructures to handling, particulates and condensation during manufacturing [4].

Bulk micromachining [5] involves etching features directly into silicon wafers or other substrates. Typically, if integrated electrical function is required the micro-electronic elements are created using CMOS processes on the top side of the silicon wafer, and then bulk micromachining commences from the other side of the wafer to yield mechanical elements such as thin diaphragms or beams on the top side of the wafer, or passages for fluid flow [1].

Molding process works to create the mechanical elements of the device by deposition of material into a microfabricated mold. The most widespread such process is ``LIGA". LIGA is a German acronym for the major process steps: Lithography, Galvanoformung (electroforming) and Abformung (molding)] [6]. The basic process consists of creating a polymer mold by lithography and then electroplating metal into the mold cavities. Micromolding processes are also used to create microstructures from materials that are difficult to etch selectively, or to create very high-aspect-ratio structures.

1.1.2. MEMS materials

Silicon is the most commonly used material in micromachining because (1) the process is well established, (2) it has good mechanical properties, and (3) integration with electronic and sensors is possible [2]. Silicon micromachining was first started at Bell Laboratories back in the 1950“s [7] where the piezoresistive effect of silicon was discovered. Other materials have also been used for specific purposes in micromachining. Fox example, Silicon carbide (SiC) exhibits excellent electrical,

mechanical, and chemical properties, making it well suited for harsh environment applications where traditional MEMS are constrained by the physical limitations of silicon (Si) [8-9]. Polymers are useful in sensing of chemical gases because of their absorption and adsorption properties [10] and polymethylmethacrylate (PMMA) is a useful polymer in the LIGA process for forming high aspect ratio structures. Special alloy materials are used for magMEMS [11]. GaAs is reported suitable for RF-MEMS [12-13].

Among a number of non-Si materials, quartz draws more attention for its excellent physical and chemical properties.

1.2 α crystal quartz

Quartz has several interesting properties [14-15] as MEMS material, some of which would effectively compensate the silicon material.

Crystallography: At room temperature, quartz has a trigonal crystal structure. This α-quartz has either a left or a right orientation structure. Above the Curie temperature of 573 ^{o}C, the structure is transformed into hexagonal β-quartz, which has markedly less piezoelectric activity. Quartz exhibits several natural crystallographic planes with a threefold symmetry around X axis, and twofold symmetry around Y axis. The crystal axis of X, Y and Z are called electrical axis, mechanical axis and optical axis, respectively.

Etching anisotropic property: Superior to quartz glass (fused silica), quartz can also be anisotropic etched. The anisotropic property is dependent on the crystal orientation. This property would give the possibility to the fabrication of high aspect ratio microstructure.

Piezoelectricity: The piezoelectric effect can be used to both excite and detect mechanical vibrations. For resonators, μW power levels suffice to sustain these vibrations. Quartz was the first piezoelectric crystal to be used widely. This natural property makes it superior to silicon for transducer applications.

Mechanical property: Quartz has high modulus of elasticity and some other mechanical strength. Our recent study further demonstrated that for microfabricated samples the tensile strength, torsional strength and bending strength are stronger than ever reported [16].

Chemical inertness: Quartz has a low aging rate since it is chemically inert and is its own oxide. It is also an almost perfectly elastic material with small internal energy losses. So, high Q value can be easily achieved. In reality, quartz can only be etched by HF-based etchant. This property would contribute to the application of chemical sensor or work in harsh environment.

UV-Transparence: Since the interaction of bimolecular with UV light is one of the most frequently employed analytical methods in the field of biochemistry, UV-transparent materials, such as quartz, are often demanded by biotechnical applications. The transparency of the material can also be important for fluid or particle handling systems where visual observation of the system's interior is of interest.

Insulator: The insulating property can be an advantage over silicon, which is semiconductor, for devices in which no leakage current must exist between the various needed metallization [17]. Further the insulating properties of quartz may be required in high voltage applications where the breakdown voltage of a standard insulating oxide is exceeded. Electrophoresis and electroosmotic pumping are two examples of such requirements.

1.3 QMEMS

QMEMS is a concept of combination of quartz material and MEMS microfabrication technologies. Although Si is the mainstream of MEMS material, quartz has its advantages as mentioned above. The drawback is the electronic circuit associated with the device is not realized on the same chip. This one-chip conception is clearly an exclusive property of silicon at the moment, but for many applications, it may not be really necessary and gives rise to very tricky compatibility problems. Especially, with

the development of packaging technology, the system in one package (SIP) concept gives more opportunity to non-Si materials.

Quartz micromachining research started from 1980s at Yokogawa Electric. Since that, a number of quartz based microdevices have been reported, such as, tuning fork resonator in 1986 [18], pressure sensor in 1993 [17], microactuator [19], optical chopper in 1995 [20], tuning fork AFM probe in 2005 [21].

1.4 Quartz MEMS fabrication process

Although quartz MEMS has also about 30 years history, compared to Si MEMS the development of QMEMS is very slow. The main reason is the lack of microfabrication knowledge, especially when the MEMS device is becoming more and more complex. QMEMS process is a real bulk process, and usually it is a double-sided process. Fig. 1.1 shows the basic process flow: (1) Washing quartz wafer; (2) Sputtering Cr/Au metal films as quartz etching mask; (3) Coating and patterning photoresist for defining device structure; (4) Etching Au/Cr metal films and removing photoresist; (5) Etching quartz; (6) Etching Au/Cr metal films.

A capacitive tilt sensor has been introduced in our previous publication [22]. As shown in Fig. 1.2., basically the sensor is composed of sensitive cantilever, mass proof and comb electrodes. For realizing such a sensor, several fabrication technologies should be developed. These are: (1) Bulk wet etching technology for high aspect ratio cantilever and gap between the movable electrode and static electrode. Current high aspect ratio etching technology is based on reactive ion etching (RIE) technology, which is an expensive process and is not appropriate for mass production; (2) Three dimensional patterning technology for isolating the left side electrode, common electrode and right side electrode and leaving metal on the high aspect ratio gap side wall, which is used for creating capacitance; In traditional lithography process, resist should be coated on the side wall of high aspect ratio gap (minimum 5 μm wide and 100 μm deep) side wall, which is difficult to be realized. A new process should be considered; (3) Side wall electrode forming technology. Current metal deposition

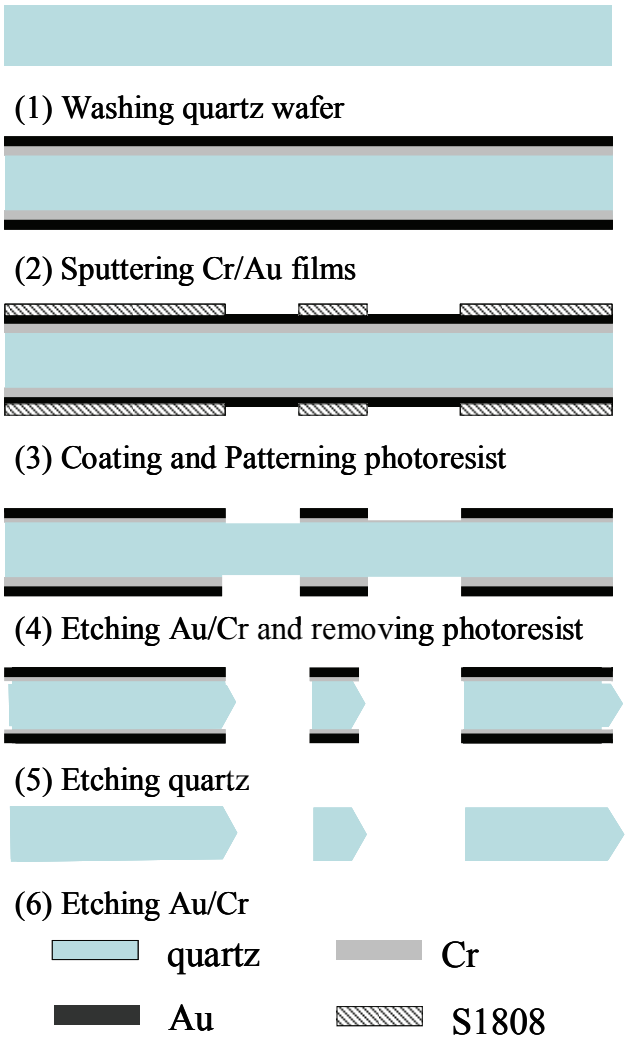

Fig. 1.1 Basic quartz fabrication process flow

techniques for improving step coverage, for example long throw low pressure deposition technique and collimator based deposition technique, suffer from the edge unbalance problem or target wasting problem. A new technique should be developed; (4) Sensor flip chip packaging technology. In traditional IC flip chip packaging, underfiller is usually used for solving the residual stress problem. However, in the case of tilt sensor (MEMS), which has movable part, underfiller can not be used. A new way should be developed for solving this problem.

This research focuses on improving such microfabrication technologies, aiming to

fabricate such a sensor, based on the basic process (Fig. 1.1.), but not limited to fabricate tilt sensor. These techniques are introduced in the following chapters.

Chapter 2 presents wet etching technology for high aspect ratio microstructures on quartz and gives some possible applications; Chapter 3 introduces a bi-layer lift-off process for patterning 3-D MEMS consisting of high aspect ratio microstructures; Chapter 4 proposes metal deposition technology for improving step coverage on the high aspect ratio microstructure side wall; Chapter 5 introduces MEMS flip chip packaging techniques and proposes a stress free packaging idea for MEMS application; Chapter 6 gives a detailed and successful application on fabricating a two-axis tilt sensor using the developed technologies. Chapter 7 summarizes the developed technologies and makes a view for further improvement.

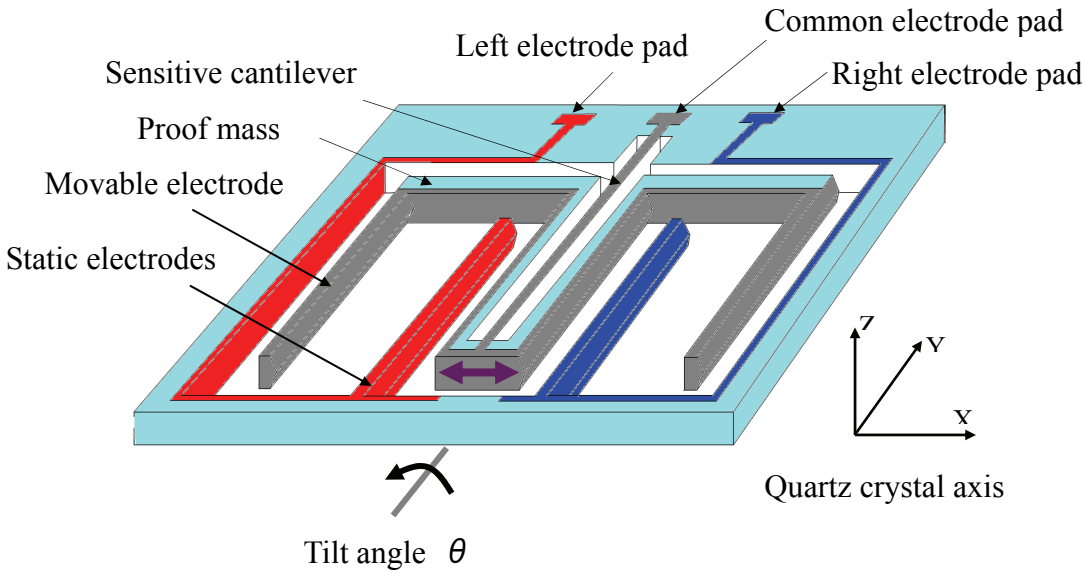

Fig. 1.2. Schematic diagram of capacitive tilt sensor

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Chapter 2 Bulk wet etching of quartz wafer

2.1. Introduction

Quartz draws great attention for its piezoelectricity, excellent mechanical characteristics and electrical insulation in comparison with the conventional MEMS material, silicon. Further, it is also well known to be the most appropriate material for bioMEMS, especially for microcapillaries because it is UV transparent and chemically inert. The major obstacles limiting the wide use of quartz wafers are its complex anisotropic etching profile and the lack of fabrication technologies.

The precise 3D microstructures with a high aspect ratio are needed in many advance applications [1]. For example, high aspect ratio microchannel would provide high sensitivity in the microcapillary electrophoresis (μ-CE) when using UV absorption detection, because absorbance is proportional to the optical path length [2]. Current CE microdevices are mostly fabricated by isotropic etching fused silica or glass, which suffer from the shallow channel depths, because the resulting channels are twice as wide as they are deep. For solving this problem, several groups have made great efforts in recent decades. Ujiie et al. [3] successfully fabricated vertical trench features with 50 μm depth and 20 μm width, the aspect ratio of 2.5, using dry etching technology. But dry etching method is an expensive process and special equipment is needed. Harrison et al. [4] reported a planar device design with an increased sensitivity, in which the measuring beam was launched through a U-cell, increasing the path length by allowing the beam to pass in a longitudinal direction along the flow channel. Unfortunately, the insertion of optical fibers into etched channels within the device made it difficult to manufacture. Further, capacitance based sensor is commonly used for acceleration, tilt detection. In this case, high aspect ratio through-hole derives big capacitance and high sensitivity.

Ueda et al. [5] systematically studied the etching anisotropy of quartz by using 21 kinds of cut angles twenty years ago, and after that Cheng et al. [6] reported characterization results of anisotropic etching properties using a spherical specimen. But

the undoubted fact is that the actual application of quartz for MEMS was very few in comparison with Si. Z cut quartz wafers show the most potential to fabricate microsensors and microactuators due to the high etch rate at the Z plane. Hedlund et al. [7] anisotropically etched z cut quartz using the mixture solution of HF and NH_4F at different concentrations, temperatures and gave the etching profiles. But the etching rates of side wall planes were not provided, which should be important in designing microdevices. This research experimentally studied wet-etching profile and etching rates of appeared etching planes using traditional quartz wafer etchant, saturated ammonium bifluoride solution at 87 degrees C. Furthermore, possible high aspect ratio microstructures were discussed and proposed and prospective MEMS applications, such as MEMS tilt sensor, microcapillary, were also introduced.

2.2. Experimental

2.2.1. Mask pattern design

Experimental mask patterns were set up with initial widths of 5, 10, 20, 50, 100 and 200 μm (Fig. 2.1.). Large width 200 μm pattern was for observing the whole etching profile and minimum 5 μm was for discussing the possible high aspect ratio microstructure [Aspect ratio = etch depth/(undercut + initial width)]. The intermediate spaces were design to observe the procedure of disappearing of etching plane. Because α-quartz is threefold symmetry, studied polar angles were limited from 0° to 120° with an interval of 5° at the beginning of +x axis.

2.2.2 Etching process and related chemicals and equipment

Notes: In the full thesis paper, if no special requirement, the chemicals preparation and process operation method are as following.

Fig. 2.2. shows the process flow.

1. Washing 100 μm thick z cut quartz wafer in $H_2SO_4 \cdot H_2O_2$ solution (3:1 at volume) at 110± 5 ^oC for 15 min. After that, wafers are removed to pure warm water at 80 ^oC for 5 min and two times followed by flowing water washing for 1 min. Finally, nitrogen drying is performed. $H_2SO_4 \cdot H_2O_2$ solution is prepared as the following

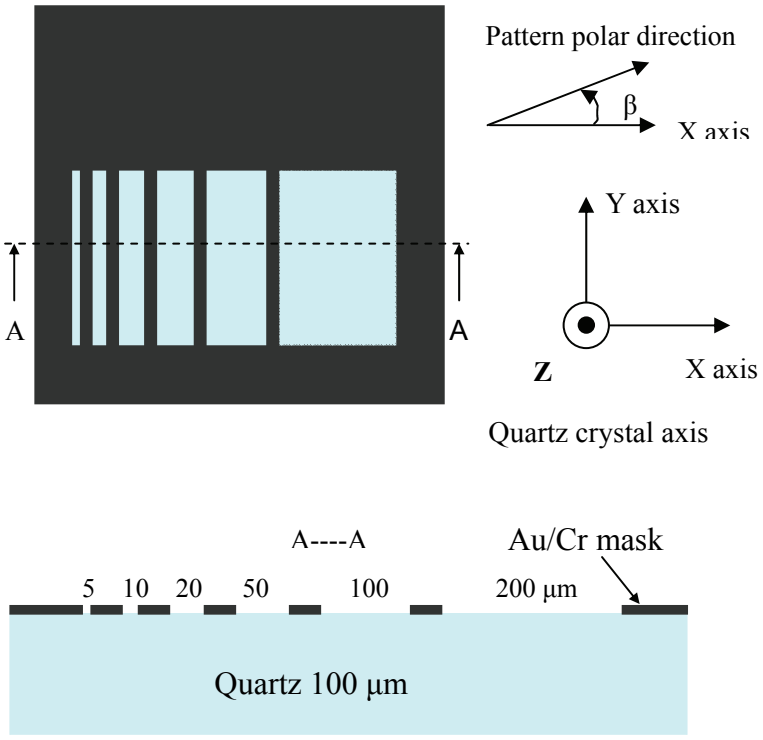


Fig. 2.1. Designed etch mask with initial spaces of 5, 10, 20, 50, 100 and 200 μm (from left to right) and definition of the pattern polar direction β starting from +X

.

procedure: (1) Pouring 200 ml hydrogen peroxide H_2O_2 (30% aqueous solution) into fused silica beaker on a hot plate; (2) Pouring 200 ml H_2SO_4 (96% aqueous solution) solution and stirring: (3) Pouring 400 ml H_2SO_4 solution; (4) Turning on the hotplate and keeping the solution at 110 ^oC.

2. Sputtering Au/Cr metal films on quartz wafers using double-sided sputtering machine Anelva SPP430H. Here Au is the real quartz etching mask and Cr is used as adhesive between quartz and gold. For preventing the oxidation of Cr film, Au should be sputtered continuously after sputtering Cr. The sputtering parameters are listed in Table 2.1. The thicknesses of Cr and Au using these parameters are 50 nm and 165 nm respectively.

Tab. 2.1. Sputtering parameters of Au and Cr

Target	Time (min)	Power (w)	Gas pressure (mTorr)
Cr	6	600	2
Au	15	400	2

3. Spin-coating resist and patterning resist. (1) Spin-coating photoresist Shipley S1808 at 4000 rpm for 20 s on the one side followed by softbaking treatment at 90 ^{o}C for 10 min in an oven; (2) After 5 min naturally cooling, spin-coating S1808 at 4000 rpm for 20 s on the other wafer side followed by soft baking treatment at 90 ^{o}C for 15 min; (3) After 10 min naturally cooling, the wafer is removed to a double-sided exposure machine Cannon BPA-200, and exposed to UV light using the designed etching mask for 10 s. (4) Developing the wafer for 60 s in Shipley developer CD-26 followed by pure water washing two times for 30 s; (5) Hardbaking the wafer at 120 ^{o}C for 30 min in an oven.

4. Etching Au/Cr metal film: (1) Selectively wet etching gold film by immersing wafer into gold etchant for about 15 s followed by pure water washing two times for 60 s each. The gold etchant is prepared by mixing KI: I_2; H_2O=200g: 50 g: 200 ml thoroughly. (2) Selectively wet etching Chromium film by immersing wafer into Cr etchant for 10 s followed by pure water washing two times for 60s each. The Cr etchant is standard product, MPM-E30.

5. Removing photoresist S1808: Resist removal is performed using warm Shipley remover 1161A solution at 80 ^{o}C.

6. Etching quartz: Quartz is etched using saturated bifluoride ammonium solution at 87±2 ^{o}C. The etchant is prepared by dissolving the HF・NH_4F chemical into warming pure water. It is surely difficult to justify the chemical is saturated or not. To my experience, when saturated a thin film on the surface will appear but the solution is

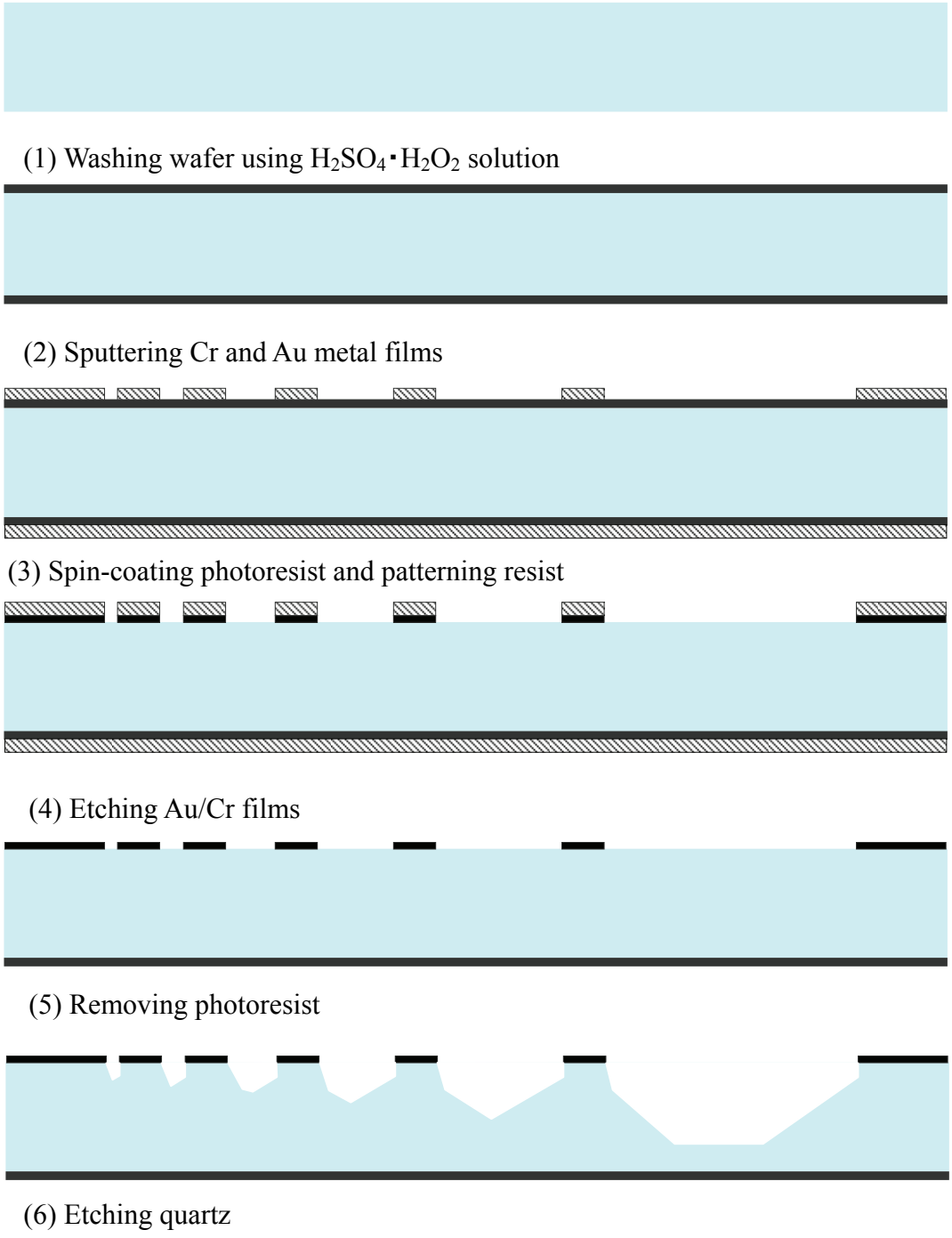


Fig. 2.2. Process flow for etching quartz

transparent. The used chemical and water were 630 g and 300 ml. In this research, a stirrer was not used and no chemicals or water were supplemented.

2.2.3 Analysis method

2.2.3.1. Definition of etching profile

After substrate etching, samples were cut vertically to the etching line and cross sections were observed using scanning electron microscopy (SEM). Etching profile was defined in Fig. 2.3.

2.2.3.2. Track of the intersection of two etching planes

The appeared etching planes would advance in parallel and the intersection of the etching planes is decided by the following formula (1) [8]. (See Fig. 2.4.)

$$R_\theta \sin\zeta = R_0 \sin(\zeta + \theta) \quad \text{.....(1)}$$

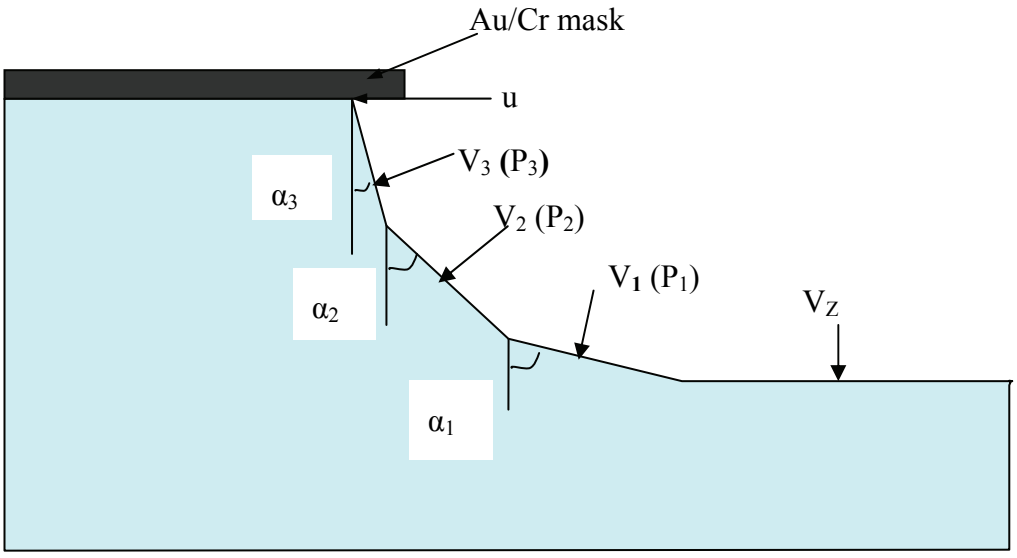


Fig. 2.3. Definition of the sidewall profile with plane P_1, P_2, P_3 and Z, and the angle α_1, α_2, α_3 and etching rate V_1, V_2, V_3, V_Z and u

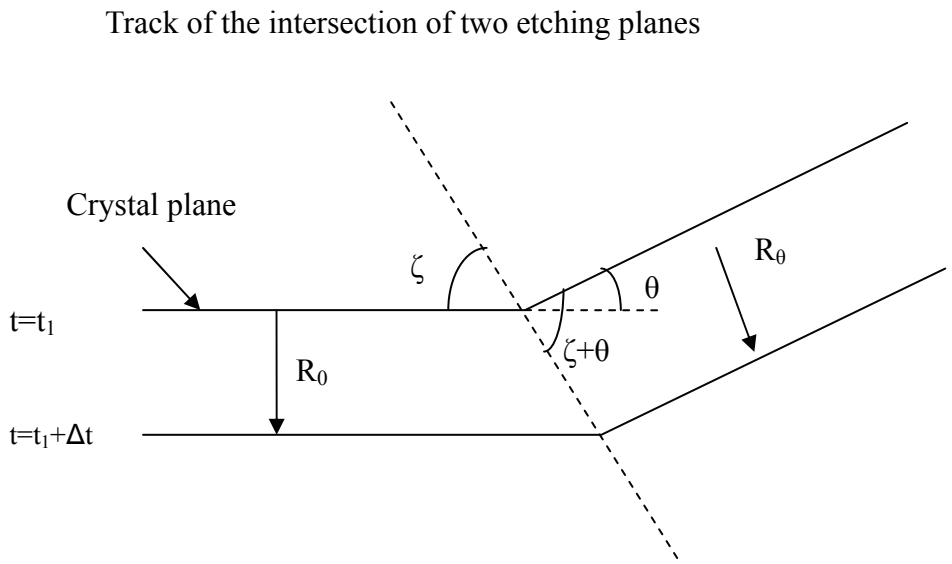


Fig. 2.4. Etching planes and the track of their intersection

2.2.3.3. Observing and calculating etching profiles

Fig. 2.5(a) shows an example of the SEM picture for measuring the etching profile. Fig. 2.5(b) gives an example picture for measuring undercut. The undercut was clearly observed at the SEM photograph (Fig. 2.5(b)), the dark and bright part represents films with and without quartz, respectively.

Based on the Fig. 2.4, the etching rates of side wall P_1, P_2, P_3 and the Z plane can be calculated by the following formula (2), (3), (4) and (5), respectively.

$$V_1 = \frac{(W_1 + U)\cos\alpha_1}{t} \quad \text{.....(2)}$$

$$V_2 = \frac{(W_2 + U)\cos\alpha_2}{t} \quad \text{..... (3)}$$

$$V_3 = \frac{U\cos\alpha_3}{t} \quad \text{..... (4)}$$

$$V_Z = \frac{D}{t} \quad \text{..... (5)}$$

V_1, V_2, V_3: etching rate of side wall P_1, P_2 and P_3 respectively

V_Z: etching rate of Z plane

U: etching undercut

t: etching time

W_1 (W_2): distance between the intersection of P_3 (P_2), Au/Cr mask and the intersection of P_1 (P_2), Au/Cr mask

2.3. Results

2.3.1 Characterization of anisotropy

The angle α_1, α_2, α_3 (in Fig. 2.3) were measured and plotted in dependence on the polar angle as Fig. 2.6(a). No minus inclination angle α was observed. More attention were paid on the angle α_3, which tended to increase from β=0° to 15° and from β=90° to 120°, but also suddenly decrease from β=15° to 30°. In a wide range from β=30° to 90°, it appeared to be nearly 0°. In fact, it was difficult to measure and discriminate the angle in this range, because no bigger than 2° was observed. The side wall etching rates of V_1, V_2, and V_3 were calculated and plotted as Fig. 2.6 (b). The etching rate V_Z was 110 μm/h, which was the same at all polar direction. So V_Z was not plotted.

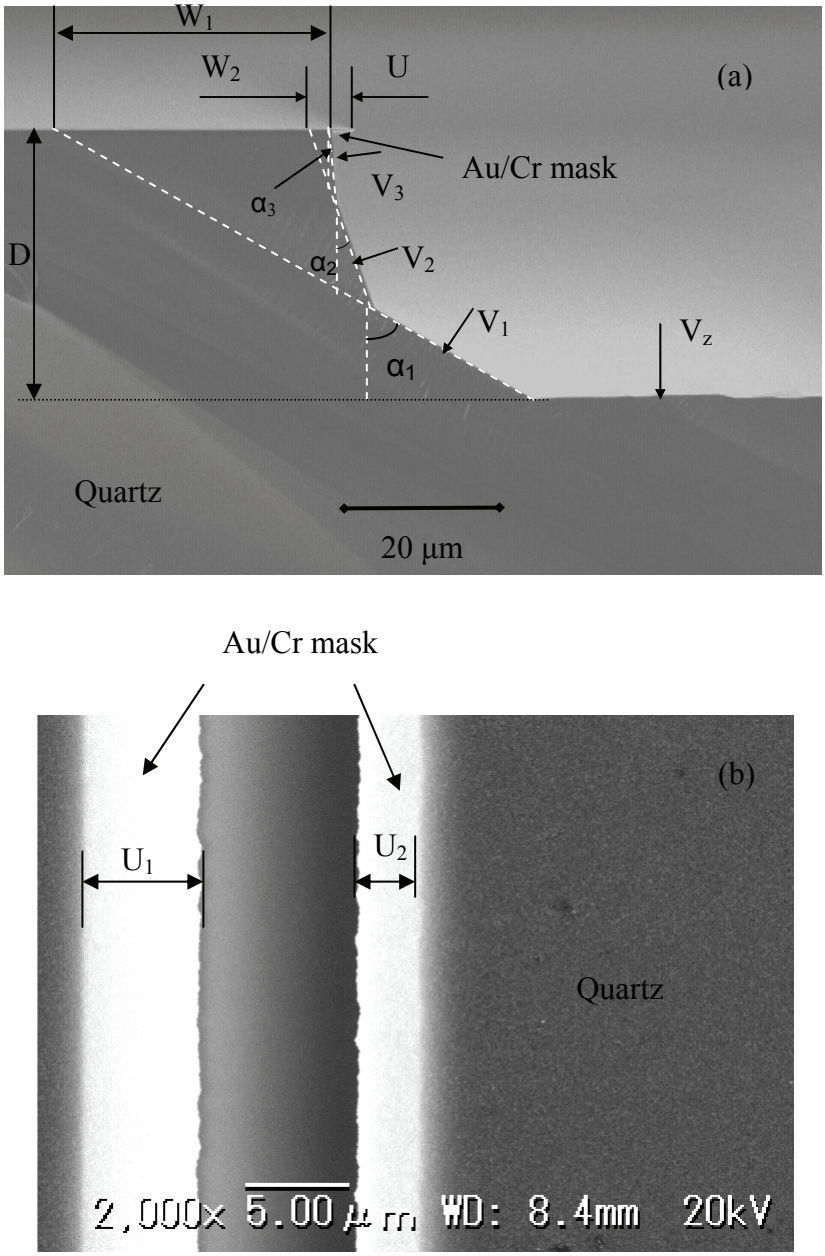
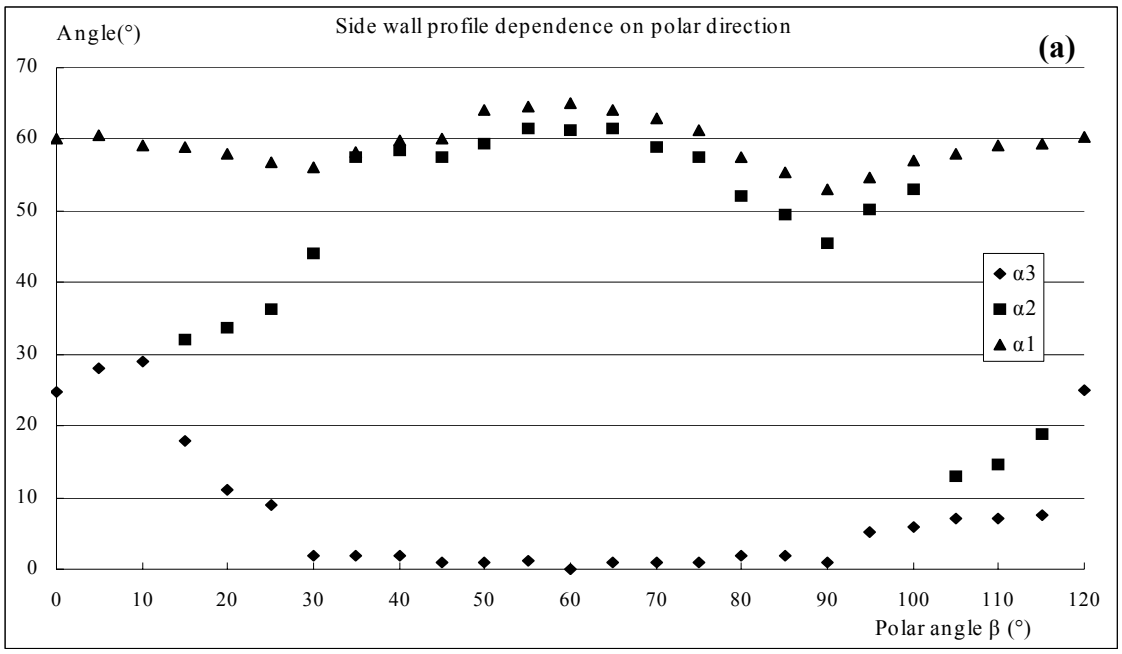


Fig. 2.5. Examples of SEM picture for measuring sidewall profiles, etching rates (a); etching undercut (b)



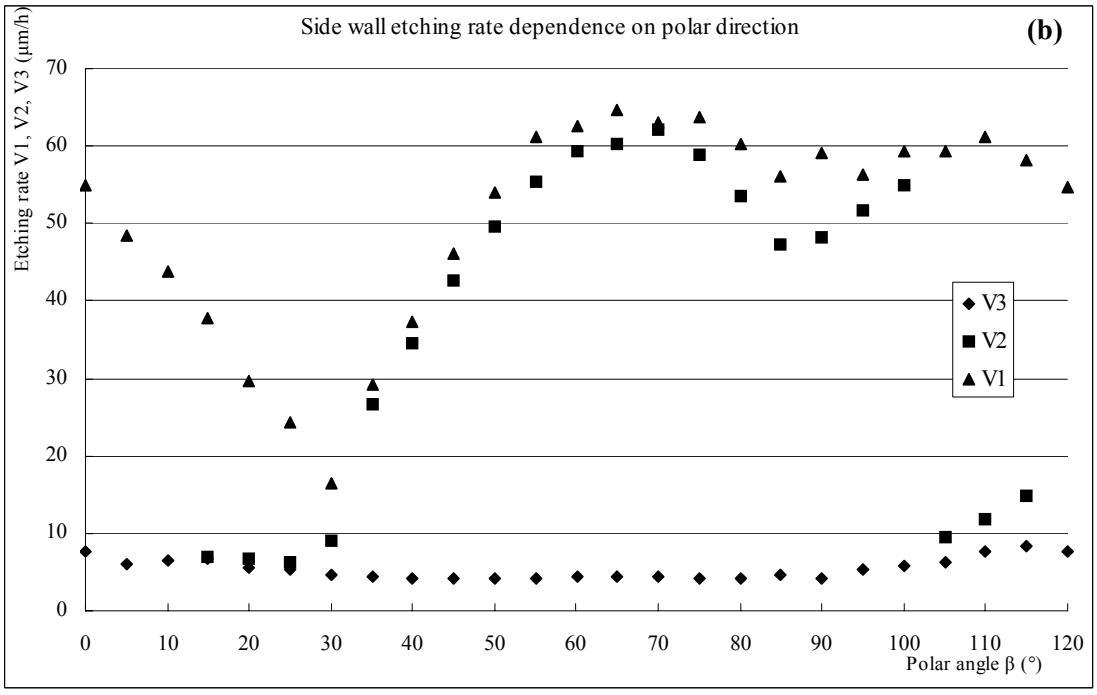


Fig. 2.6. Plotted etching profiles dependence on polar angle. Side wall inclination angle (a); Etching rate (b)

2.3.2. Trench profile dependence on initial width and etching time

Fig. 2.7 shows the typical SEM pictures including all initial widths (5, 10, 20, 50, 100 and 200 μm) .These SEM pictures were used to study high aspect ratio microstructures.

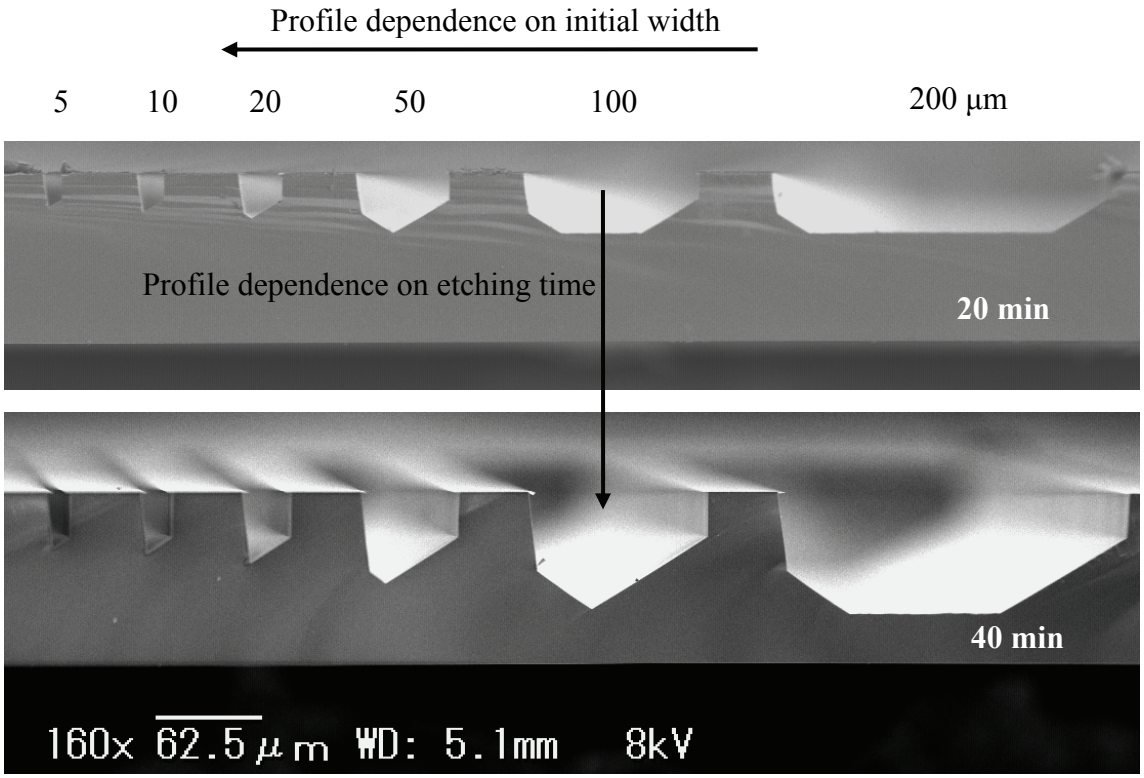


Fig. 2.7. SEM pictures of polar angle at 40° for observing the trench profile dependence on initial width and etching time

2.3.3. High aspect ratio microstructures

For MEMS applications, high aspect ratio microstructures are required in microdevices design. Aspect ratio was defined as depth/width. Structures at polar angel β should have a opposite shape with at polar angel β+60° because of the threefold

symmetry property. So trench structures were discussed from β=0° to 60°. 40 min etched results are presented in Fig. 2.8.

According to the 40 min etching results (Fig. 2.8), the basic microstructure was defined as it is presented in Fig. 2.9 (a). The 20 min, 40 min and 70 min etched results with initial width 5 μm were plotted in Fig. 2.9 (c). The aspect ratio did not arise as the increase of etching time due to the disappearing of Z plane, P_1 or P_2 as shown in Fig. 2.7. Based on the 40 min results shown in Fig. 2.8, the trench profiles can be classified as (1) β=0° to 15° , in this range Z plane and P_1 disappeared rapidly and high aspect ratio structure can not be achieved because of the big angle α_3 (Fig. 2.6 (a)); (2) β=15° to 30°, P_2 plane appeared as bottom surface, but still no high aspect ratio structure can be achieved because of the low etching rate of V_2 (Fig. 2.6 (b)); (3) β=30° to 45°, α_2 increased gradually, but V_2 increased quickly. So high aspect ratio microstructure can be achieved in this area; and (4) β=45° to 60°, V_2 became bigger, but attention should be paid to the side B, where α_2 appeared gradually, and α_3 became bigger. At β=60°, feature was achieved and returned to the β=0° feature. Fig. 2.9 (b) was an example SEM picture of 70 min etched trench with initial width 5 μm at β=45°.

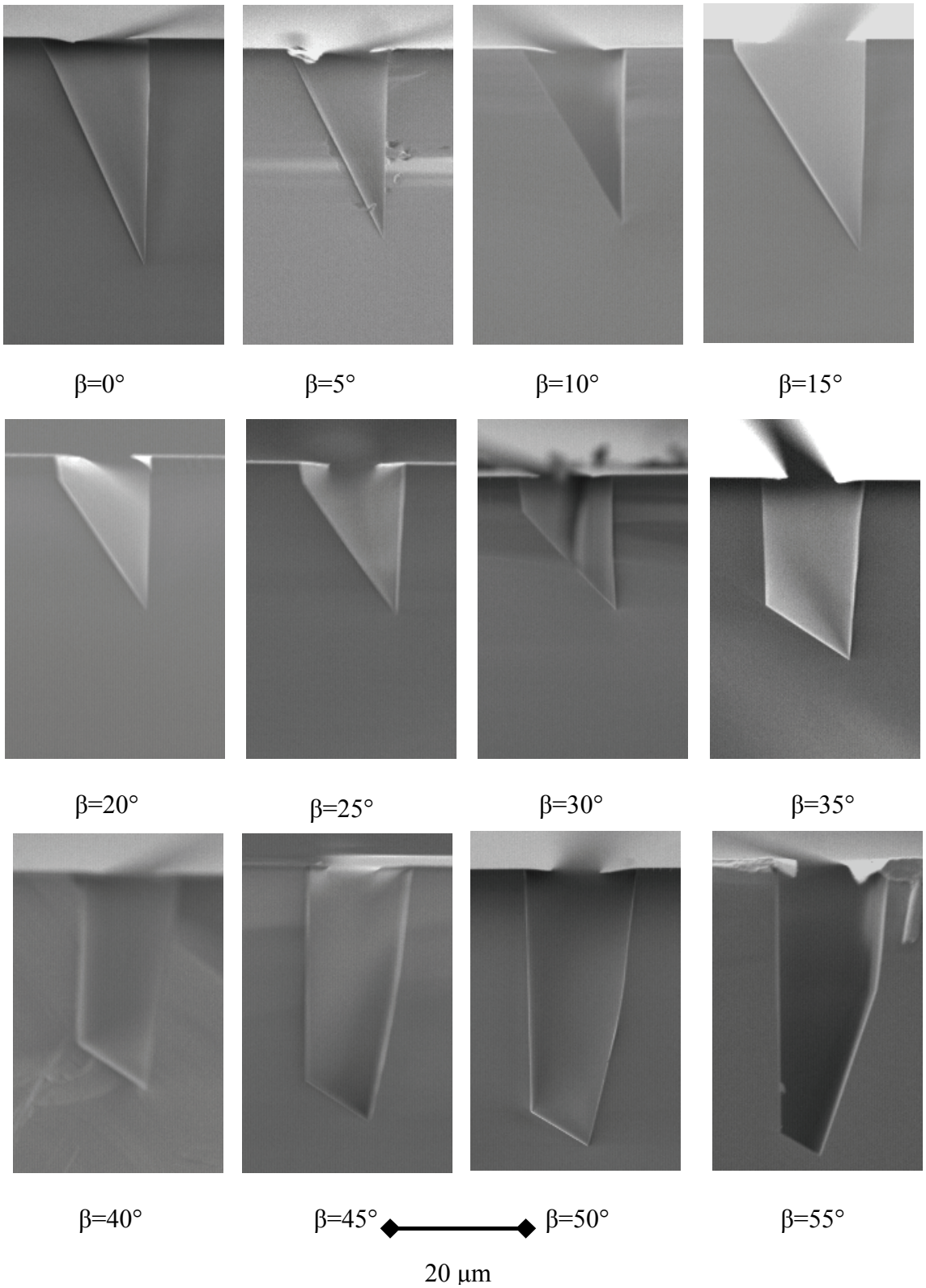


Fig. 2.8. Cross section SEM pictures from β=0° to 55° for 40 min etching with an initial width of 5 μm

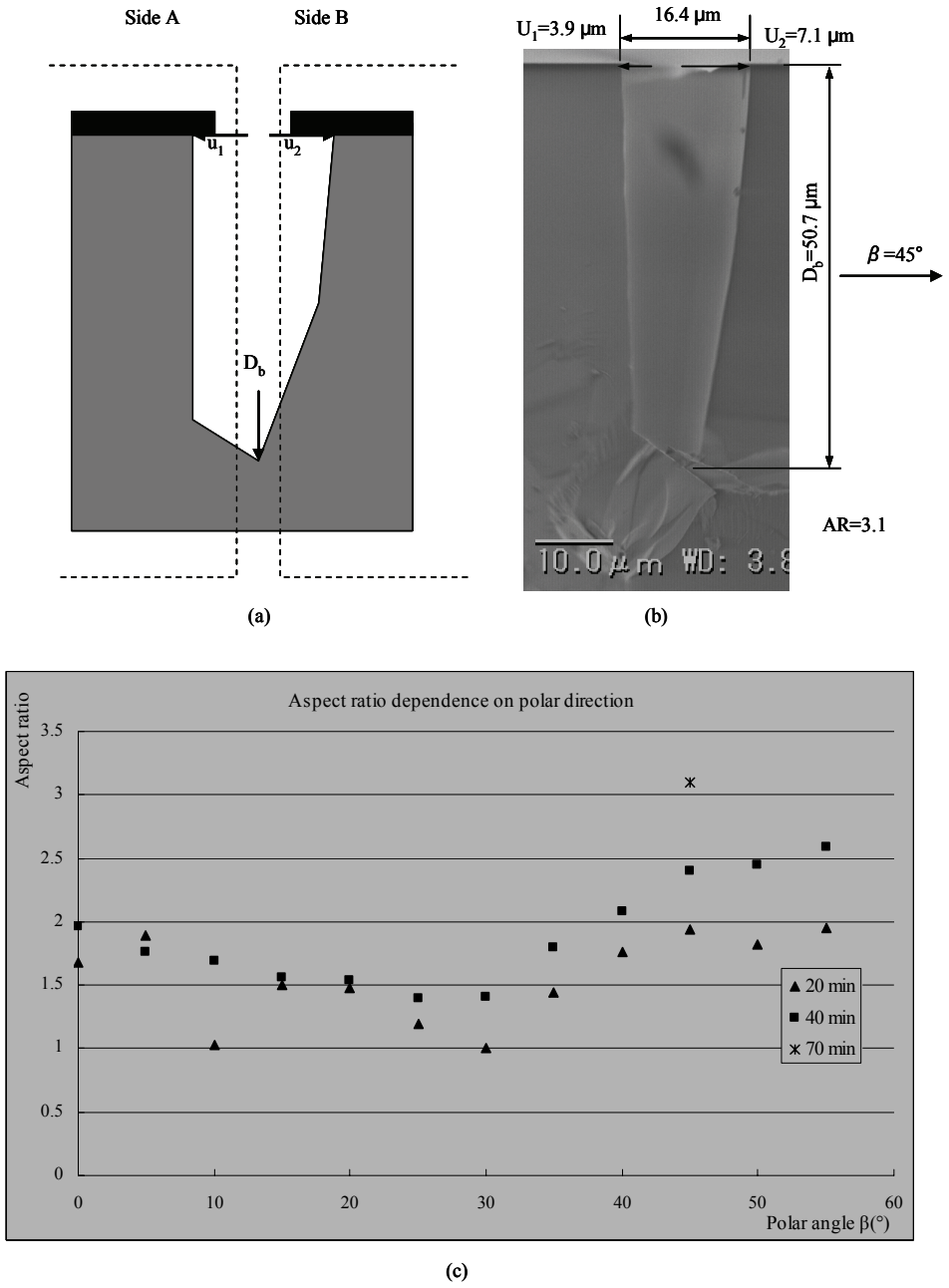


Fig. 2.9. Definition of the basic microstructure and aspect ratio: (a) the basic microstructure, u_1, u_2, and D_b represent side etch and etch depth respectively; (b) SEM photograph of 70 min etched trench at 45°; (c) Plotted trench aspect ratio [$AR=D_b/(\text{initial width} + u_1 + u_2)$] dependence on the polar direction based on the 20, 40, 70 min etching results

2.4. **Discussion and applications**

Double-sided etching experiment was also performed using the same mask pattern. The result showed that the bottom side has the same etching profile at the opposite polar direction (β) due to the twofold symmetry in the positive X axis (Fig. 2.10).

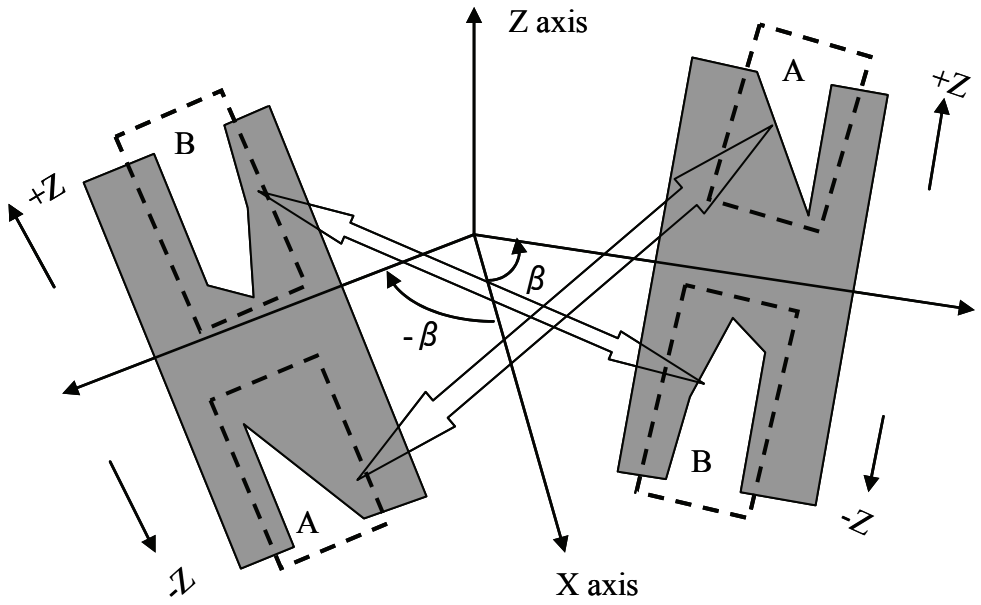


Fig. 2.10. The twofold symmetry around X axis

2.4.1 Application for microcapillary

In the case of microchannel for micorcapillary, rectangular channel should be ideal, because slope side wall decreases the UV light pass length, resulting in low sensitivity. Considering the side etching (u_1, u_2), side wall slope α, and bottom surface etching rate V_2, β=45° should be the best choice. Fig. 2.9 (b) shows the 70 min etched trench with an aspect ratio of 3.1 at β=45°.

2.4.2 Application for capacitive tilt sensor

For capacitance based sensor, quartz wafer should be etched through for achieving

movable part and static part, so called comb-electrode. The key feature of this kind of sensor is to fabricate high aspect ratio through-hole, which is used for constructing variable capacitor. Double-sided etching technique shows great interest for the twofold symmetry. A tilt sensor has been developed [9] using +X direction (β=0°) for the high etching rate of V_1 (both sides of up and down) and simple side wall profile (up-down symmetry). The sensor is composed of comb-electrode, mass proof and long elastic cantilever. Fig. 2.11 shows the pictures of the fabricated tilt sensor. In general consideration, for designing two-axis sensor on one chip, sensor 2 will be arranged 120°

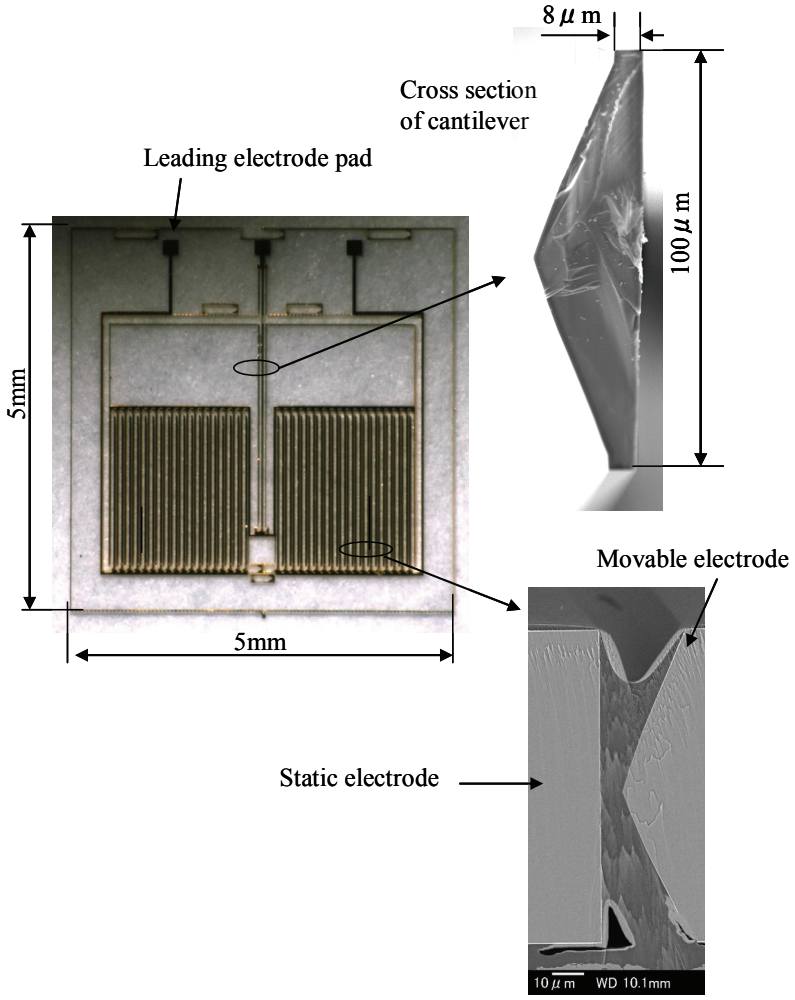


Fig. 2.11. Fabricated capacitive tilt sensor using +X direction through hole

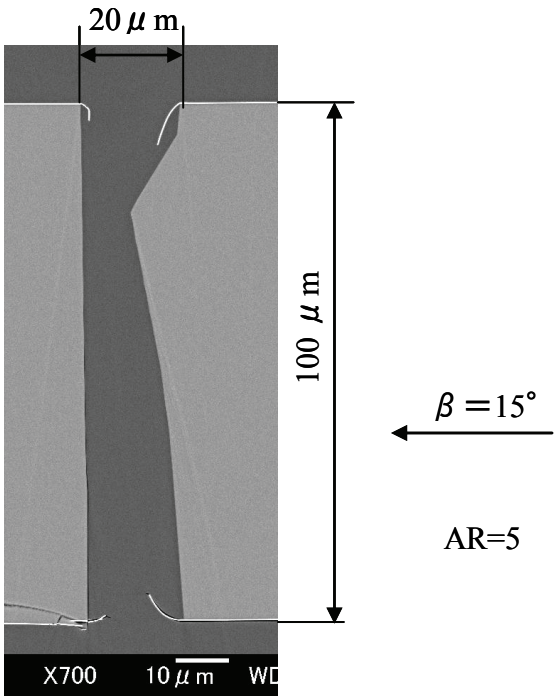


Fig. 2.12. Cross section of double-sided etched high aspect ratio (AR=5) through hole at β=15°, 90 min

to the sensor 1 (+x direction) for the well-known threefold symmetry property. However, 90° arranged two axis sensor should also be achieved, if letting β satisfy the following formula (6) taking advantage of the twofold symmetry around X axis (Fig. 2.10).

$$\beta - (-\beta) = 90^{\circ} \quad (6)$$

Namely, at β=45° and -45° same two sensors can be achieved, which just have up-down counter etching profiles. Further, considering the threefold symmetry property, two same sensors can also be achieved if satisfying the following formula (7), which gives β=15°, arranging two sensors at β= 15° and 105° (-15°+120°).

$$120 - \beta - \beta = 90^{\circ} \quad (7)$$

Actually, through-holes at β=45° and 105° have the same etching profiles, which are only left-right counter. In conclusion, there is only one kind of through-hole etching

profile which can be used for fabricating 90° arrangement two axis tilt sensor. Fig. 2.12 shows the cross section of double-sided etched high aspect ratio through-hole at β=15°, which was etched with an initial width 5 μm for 90 min.

For deep wet etching quartz, high quality protective mask is needed [10-13]. Au/Cr is commonly used quartz and glass etch mask. The first thin Cr layer is to enhance the adhesive strength between gold and substrate. Pinholes and notch defects are the notorious problem when using Au/Cr mask in HF etchant. The residual stress in the mask layers is responsible for the pinholes and notch defects due to the breakage of highly stressed mask layers during the etching process [14]. The Au/Cr mask quality can be improved by optimizing film deposition condition. Fig. 2.13 gives a failure example of masking after 15 min quartz etching. Gold layer peeled off. By changing the sputtering conditions, this problem was solved. Tab. 2.2 shows the improvement of sputtering conditions.

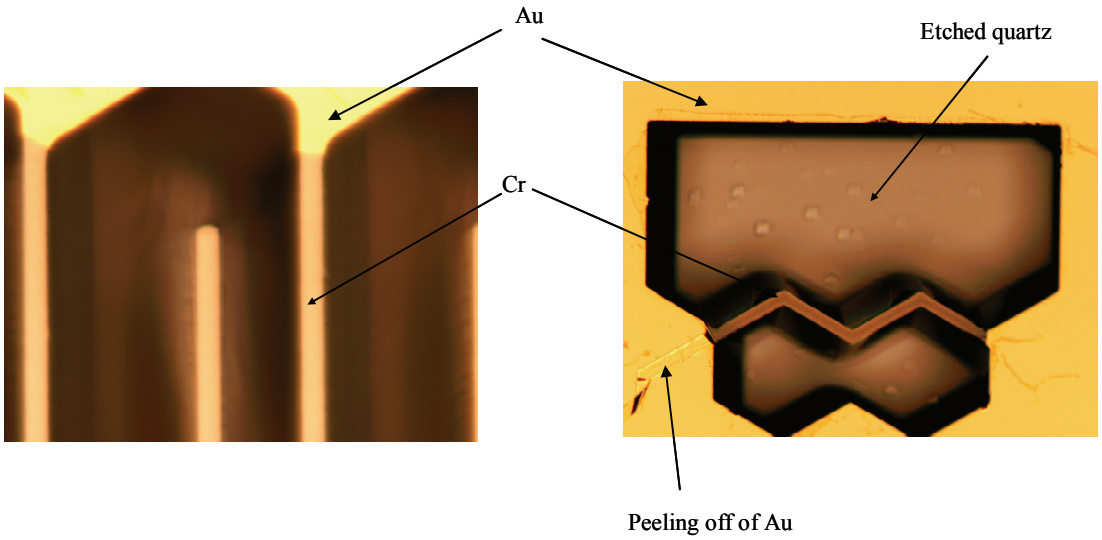


Fig. 2.13. An example of failure Au/Cr masking

Tab. 2.2 Comparison of failure and success sputtering conditions

Sputtering condition	Failure		Success	
	Cr	Au	Cr	Au
Power (w)	600	200	600	400
Pressure (mTorr)	5	5	2	2

The improvement is based on the following issues: (1) Low chamber pressure increases the mean free pass of target atom and decreases the chance of collision; (2) Dense films can be achieved in low pressure [14]; (3) High power for Au increases the adhesive strength between Cr and Au; (4) Low chamber pressure and high power decrease the residual stress. However, the relationship between sputtering conditions and residual stress is not clear, because it is also dependent on sputtering equipment. For deeper etching and finer pattern requirement, it is worth to investigate the relationship between sputtering conditions and residual stress.

2.5. Summary

High aspect ratio microstructure (> 3) which was considered impossible by wet etching technology [3] was achieved. This result suggests that anisotropic etching of Z cut α-quartz can be applied to microcapillary electrophoresis, where high aspect ratio microchannel is desired for improving detecting sensitivity. The dependence of aspect ratio on polar angle would give important guidance to the design layout. Trench at polar angle of β=45° is demonstrated to be the best choice. Nearly vertical trench feature was fabricated at β=45° with 50.7 μm depth and 16.4 μm width, the aspect ratio of 3.1. Double-sided etching showed great interest for the twofold symmetry around the X axis. According to this property, two same sensors at (β=15° and 105°) and (β=-45° and 45°) can be arranged at 90° on one quartz chip, which propose a novel two axis tilt sensor [15-16].

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Chapter 3 Bi-layer lift-off process for 3-D patterning

3.1. Introduction

3.1.1. Traditional photolithograph process for 3-D patterning

In traditional photolithograph process, resist needs to be coated on the sidewalls of a high aspect ratio trench or a through-hole to define a three 3-D (three dimensional) microstructure pattern. In general consideration, for establishing a pattern like Fig. 3.1 (6), process should be designed as shown in Fig. 3.1: (1) Depositing film A on substrate as substrate etching mask; (2) Spin-coating photoresist and creating resist pattern; (3) Etching film A and removing resist; (4) Depositing film B for final electrical pattern; (5) Recoating resist on the etched 3-D microstructure and creating resist pattern; (6) Etching film B and removing resist. However, it is difficult to coat resist on the vertical sidewalls of high aspect ratio microstructures. Spray coating system has been reported for deep structures [1], but successful resist coating on the sidewall of a through-hole at high aspect ratio has not been found. Electroplatable photoresist such as Shipley ED2100 has been recently introduced [2]. In the case of bulk etched MEMS device including movable part, stiction problem should be a negative concern, because it would hinder the photoresist plating.

3.1.2. Lift-off process

Lift-off is a patterning technique that is widely used for defining very fine pattern or removing hard-etched metals such as platinum [3-5]. The basic principle of the process is as Fig. 3.2. Lift-off is a technique using reverse pattern. During the actual lifting-off, the photoresist under the film is removed with solvent, taking the film with it, and leaving only the film which was deposited directly on the substrate. In detail, (1) Creating a resist pattern with an overhang profile (undercut); (2) Directionally depositing metal film on the resist and substrate, overhang structure would separate the deposited metal films on and under resist; (3) Etching the resist with remover,

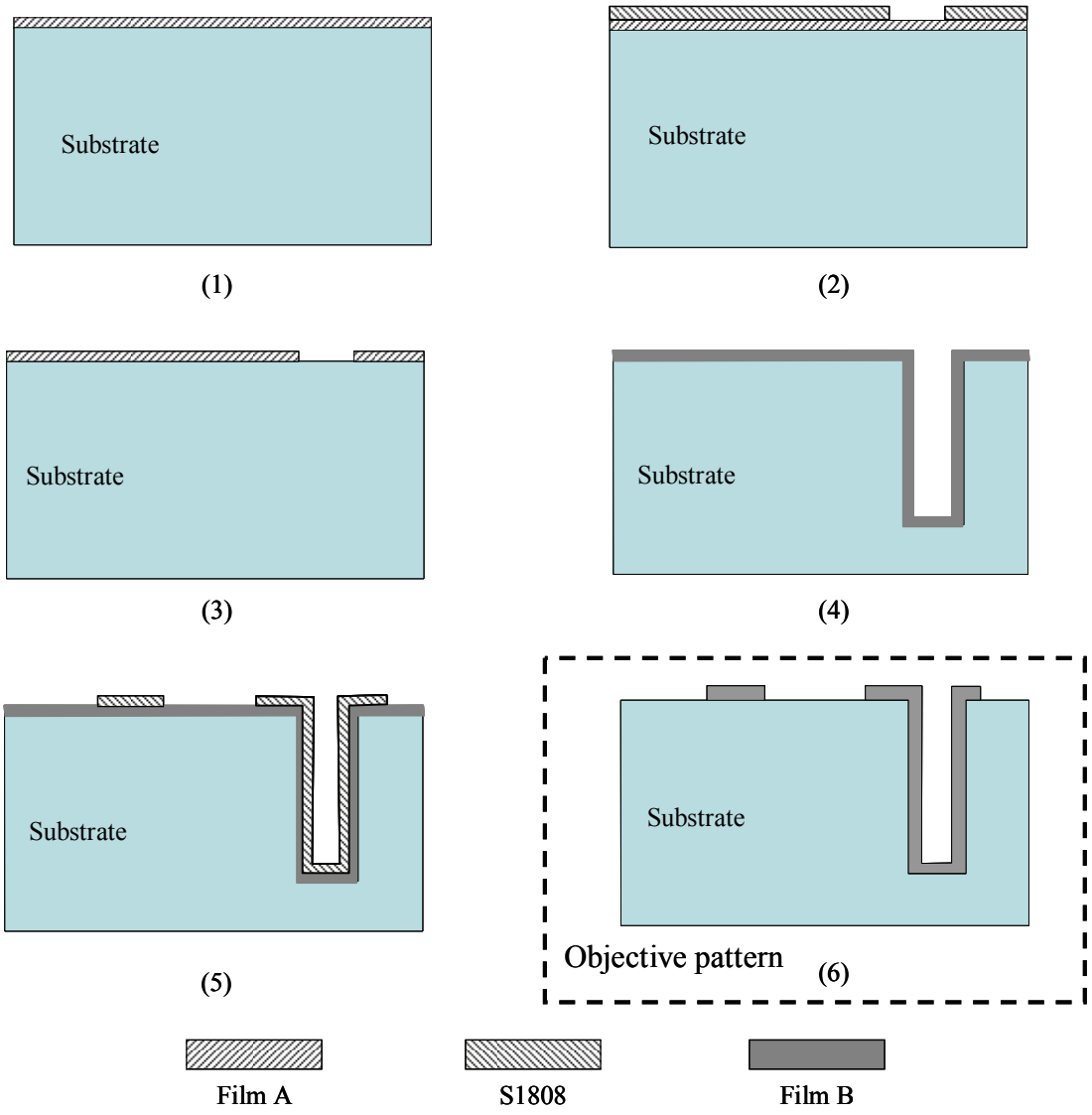


Fig. 3.1. Patterning 3-D microstructure using traditional lithograph process

consequently lifting-off the unwanted metal films on the resist. The key feature of the process is to create an overhang resist profile for separating the wanted film and unwanted film. There are mainly two methods to create an overhang profile. One is surface modified photoresist processing, which is a single-layer method. The top surface of the photoressist can be chemically modified to develop at a slower rate than the underlying resist. The chemical treatment is typically by soaking the resist in chlorobenzen or toluene solution, either before or after exposure but prior to

development. This method is simple but suffers from the bad reproducibility and the chemicals are not environmental friendly. The other method is LOL2000 processing, which is a bi-layer process. LOL2000 is an inert, non-UV-sensitive polymer, which can be etched with most standard photoresist developers. The LOL2000 is first spun on the substrate and pre-baked, and then the standard photoresist is spun on and pre-baked. After the photoresist is exposed as usual, the substrate is developed. The developer will clear the exposed photoresist areas, but still also etch away the LOL2000, leading to undercutting of the photoresist. The later method has become the mainstream process in present manufacture for its simplicity, good reproducibility and high tunability.

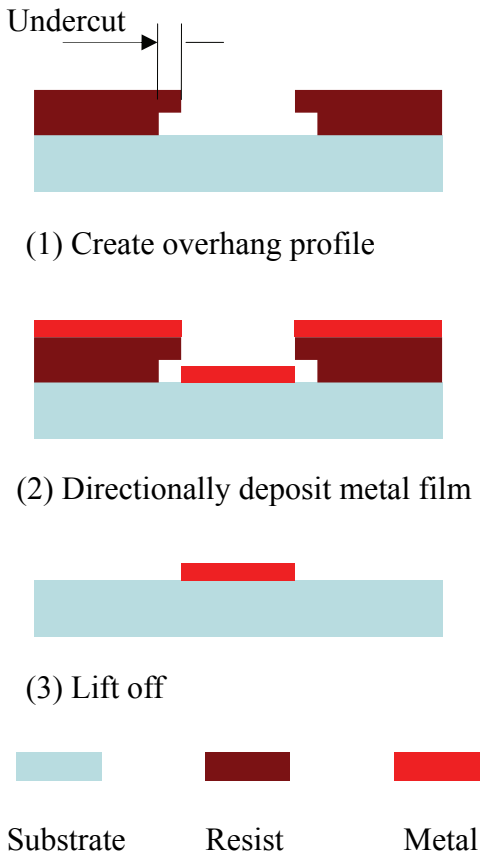


Fig. 3.2. Schematic flow of lift-off process

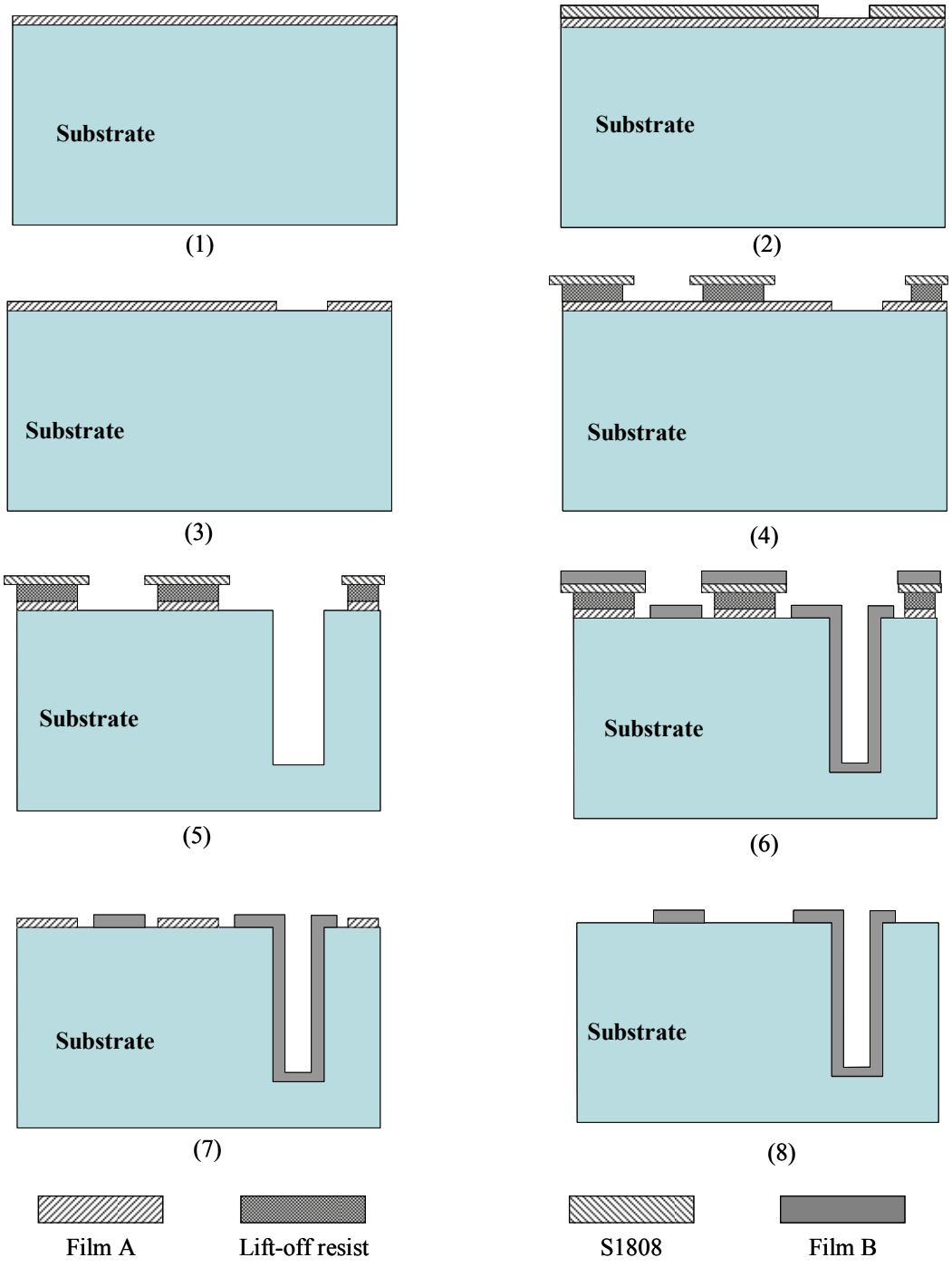


Fig. 3.3 Proposed lift-off process for 3-D patterning

3.1.3. Proposed lift-off process for 3-D patterning

Conventional lift-off process needs directional deposition, so it is limited to surface microfabrication. When the step coverage is required in 3-D MEMS, the lift-off process needs to be improved. Here a new bi-layer lift-off process is proposed for new applications on 3-D patterning, which need not resist coating after etching substrate. The process flow of the new lift-off process is shown in Fig. 3.3. (1) Depositing film A on substrate as etching mask; (2) Spin-coating photoresist and creating resist pattern for the basic 3-D microstructure; (3) Etching film A and removing resist; (4) Creating lift-off resist pattern for the final film b pattern; (5) Etching substrate and etching film A, the part of which is not protected by the resist; (6) Depositing film B on the etched 3-D microstructure; (7) Lifting-off; (8) Etching film A which was protected by the lift-off resist.

Compared to the conventional lift-off process, some additional requirements to the overhang structure should be noted. These are a deep (high aspect ratio) undercut and durable overhang which should be resistive to the aggressive substrate etchant. Because a small overhang will result in continuous film (Fig. 3.4) because of the step coverage requirement of the 3-D structure, consequently unavailable lift-off. The following sections will introduce the optimization of the process through experiment and give an application example of fabrication result of capacitive tilt sensor.

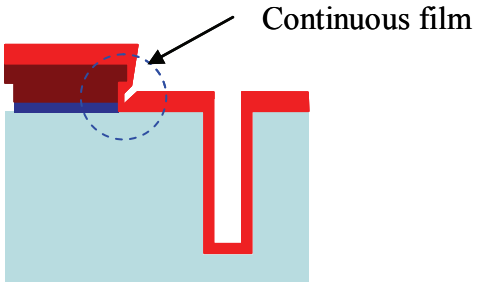


Fig. 3.4. Failure example caused by the small undercut

3.2. Creating undercut profile

There are several variables that can be used to give the desired undercut, such as exposure, soft-bake temperature and time, developer type. In this research, the resist development time was adjusted to control and optimize the process.

3.2.1 Standard method (one-step development method)

Undercut profile was created using bi-layer procedure. Detailed experimental flow is shown in Fig. 3.5. The substrate was z cut quartz wafer (100 μm) which was washed and sputtered with Cr/Au films; (1) Lift-off resist LOL2000 (Shipley) was spun on the quartz substrate at 4000 rpm for 30s and softbaked in an oven at 150 ^{o}C for 30 min; (2) Photoresist S1808 (Shipley) was spun on at 4000 rpm for 20s and then softbaked in an oven at 90 ^{o}C for 15 min; (3) The substrate was exposed to UV light for 10s; (4) Development was performed using CD-26 developer (Shipley) at 30s, 45s, 60s, 75s respectively. For enhancing the overhang resistivity to the aggressive substrate etchant, developed substrates were hardbaked for 30 min at 120 ^{o}C and 150 ^{o}C , respectively.

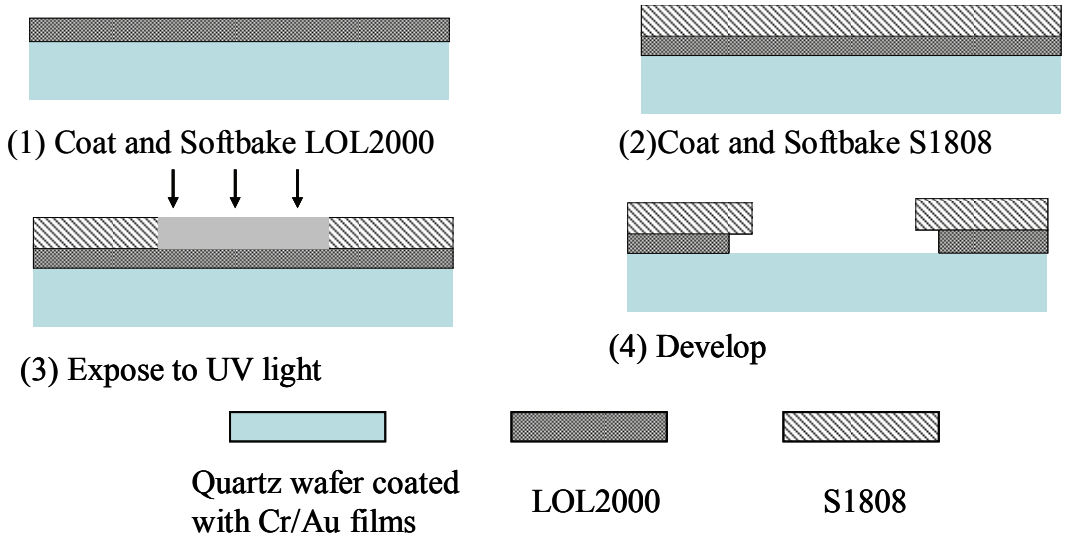


Fig. 3.5. A bi-layer lift off process for creating undercut

Fig. 3.6 gives the developed and hardbaked results. Development at 30s appears to be not enough even with resist residue. Development at 45s removed the exposed area but no undercut appeared. Development at 60s gave an undercut but the overhang was too small to reduce the step coverage. Development at 75s gave a large overhang, however, unfortunately, the overhang sagged down due to the soft photoresist (Fig. 3.6(4)). The overhang deformation was also demonstrated by the further hardaking treatment (Fig. 3.7). These results indicate that the standard one-step development method can not produce our wanted overhang, deep undercut and high resistivity. For achieving these goals, the process for creating overhang should be improved.

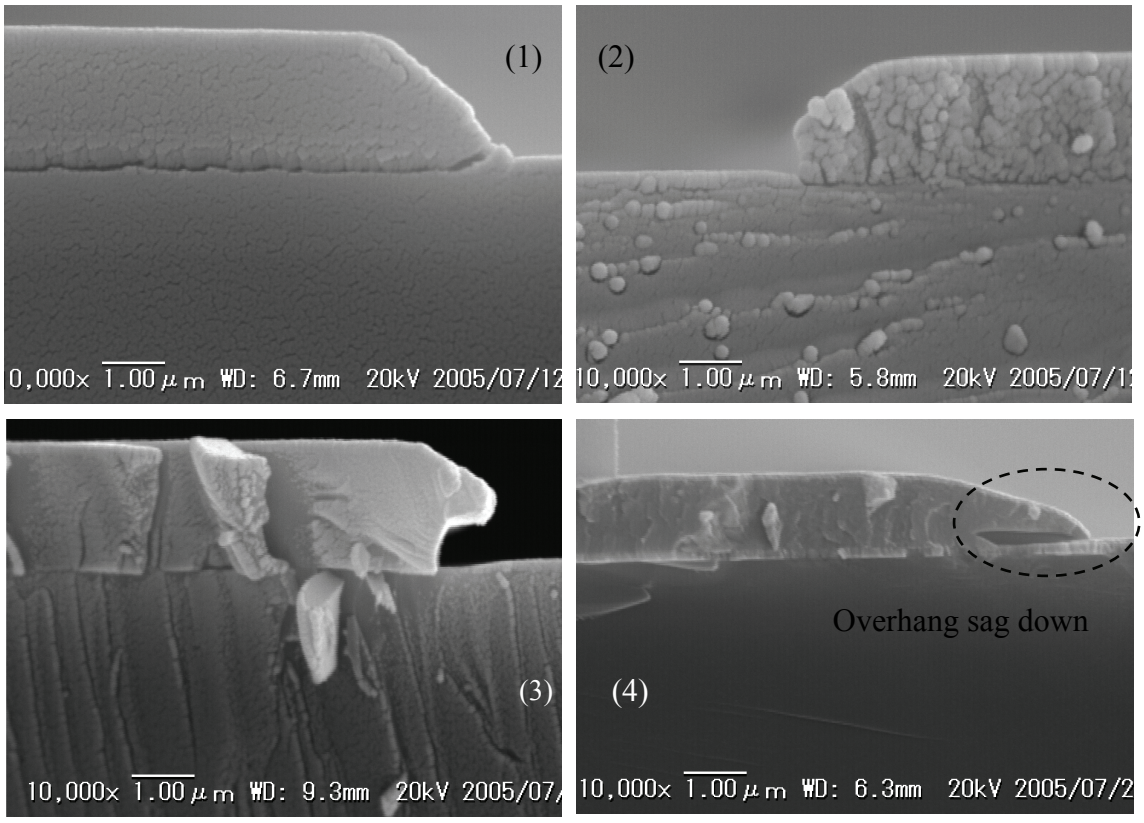


Fig. 3.6. SEM pictures of the cross section of developed results: (1) 30 s; (2) 45 s; (3) 60 s; (4) 75 s

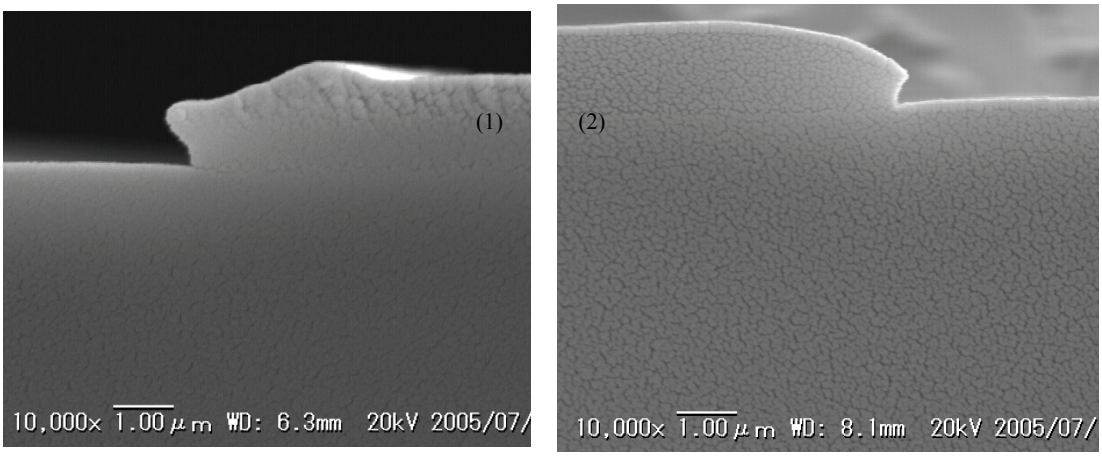


Fig. 3.7. Overhang deformation caused by hardbaking treatment for 30 min: (1) at 120 ^{o}C; (2) 150 ^{o}C

3.2.2 Improved method (two-step development method)

For solving this problem, a two-step development method is proposed. The basic consideration is to hardbake the photoresist. This treatment is expected to harden the photoresist for avoiding overhang dropping off and improving resist performance to substrate etchant. It has been demonstrated that overhang can not be hardbaked. Our solution is to arrange the hardbaking treatment before the overhang appears and after the exposed photoreisit area is removed. That is the two-step development method. By the first step development, exposed photoresist is removed but no undercut is wanted. This is for giving an opening to the second step development to the bottom lift-off resist LOL2000. After that, the substrate is hardbaked. Detailed process is shown as Fig.3.8. (1) Coat lift-off resist LOL2000 at 4000 rpm and softbake at 150 ^{o}C for 30 min in an oven; (2) Coat photoresist S1808 at 4000 rpm and softbake at 90 ^{o}C for 15 min in an oven; (3) Expose the photoresist to UV light for 10 s; (4) Develop the substrate in CD-26 developer for the first step at room temperature; (5) Hardbake resists at 150 ^{o}C for 30 min in an oven; (6) Develop the substrate in CD-26 developer for the second step

at room temperature.

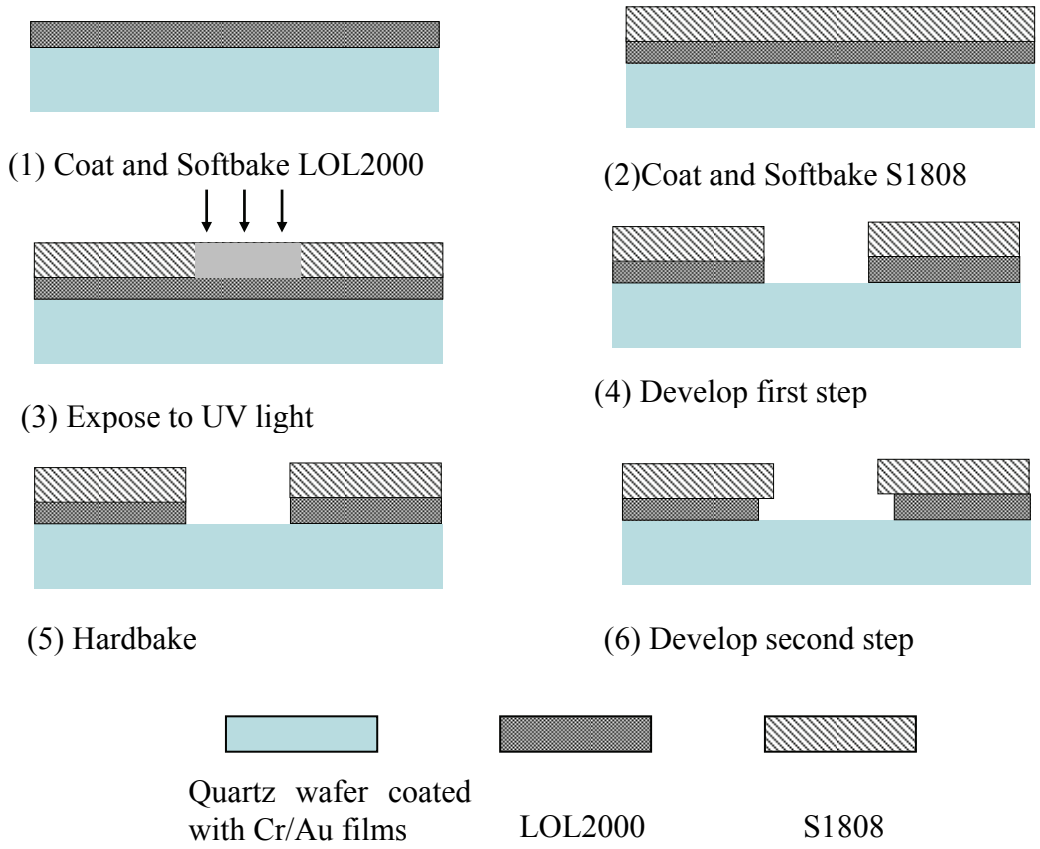
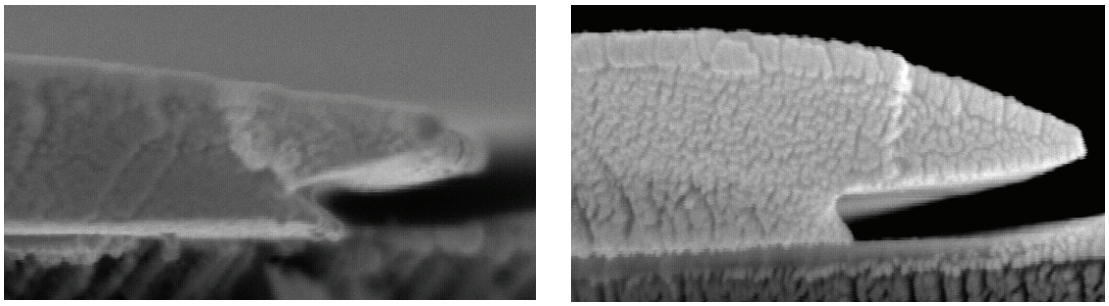


Fig. 3.8. Schematic process flow of two-step development method

The ideal profile of the first step development is thoroughly etching the exposed area photoresist and LOL but no overhang (undercut length), because resist residue will affect the second step development. If overhang happens, the photoresist may sag down or deform during the post-development hard-baking treatment, hindering the second step development. According to the standard method results (Fig. 3.6), 45s is selected as the first step development time. The second development is performed at 30s and 45s. Fig. 3.9 shows the second development results. Both results demonstrated that deep undercut can be achieved. These results should thank to the hardbaking treatment. Because deeper undercut means easier lift-off, 45s is selected as the second

development time. The performance to substrate etchant will be examined in the next section.



30s 45s

Fig. 3.9. Results of the second step development

3.3. Applications

3.3.1. Quartz MEMS based capacitive tilt sensor

Quartz MEMS based capacitive tilt sensor has been introduced in chapter 2. For patterning the leading wire and pads and electrically separating the common electrode left side electrode and right side electrode, in general consideration one should coat resist on the high aspect ratio gap side wall between movable electrodes and static electrodes. And one should be noted that the minimum gap is 5 um and the wafer thickness is 100 um, and further attention should be paid to the smart microstructure which is easily destroyed after being etched. For these reasons, efforts were made to fabricate the sensor using the proposed lift-off process and examine the effectiveness of this process [10].

Fig. 3.10 shows the detailed fabrication process, all processed are on double-sided.

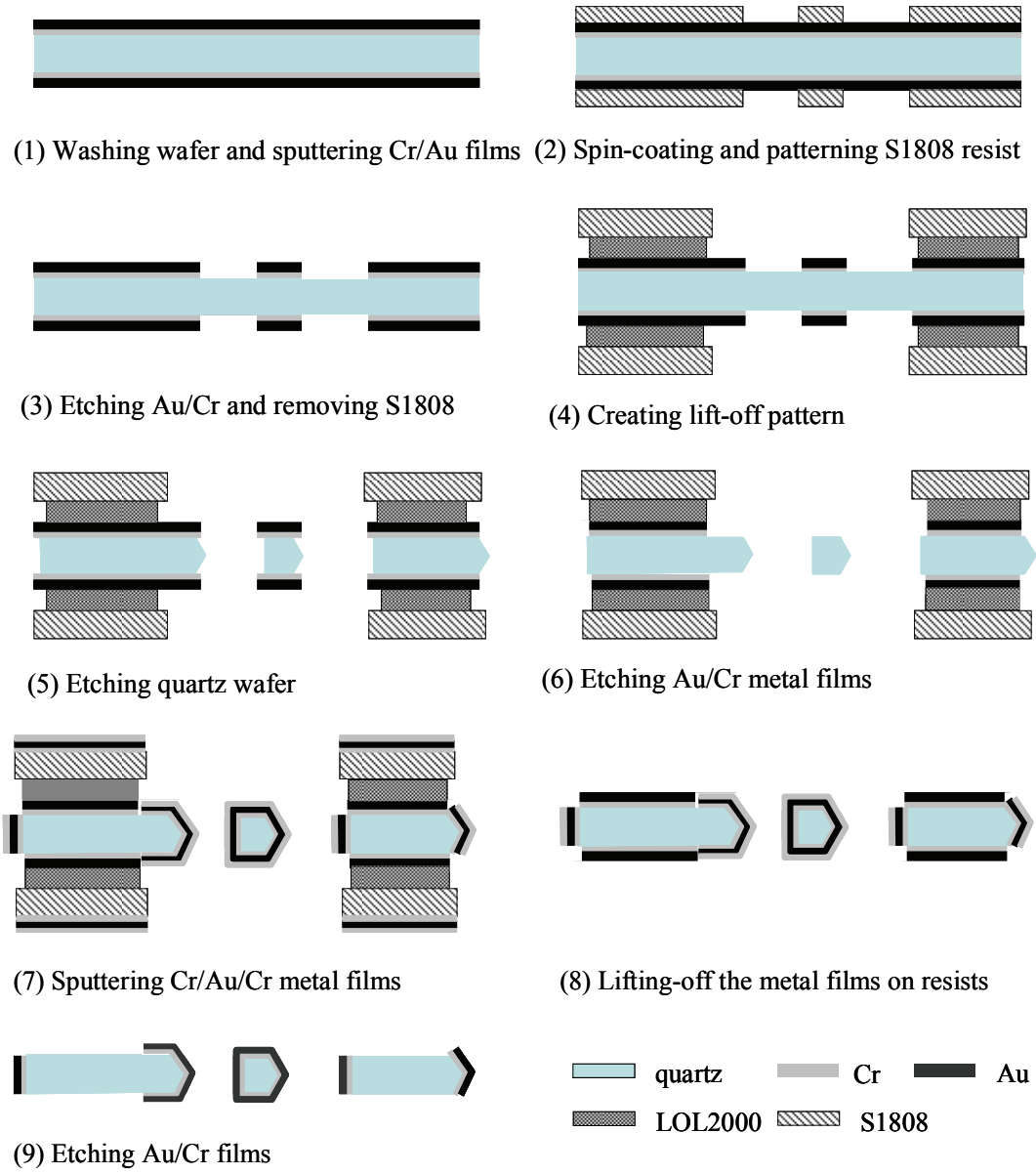


Fig. 3.10. Lift-off fabrication process for tilt sensor

(1) Washing 100 μm thick quartz wafer using $H_2SO_4 \cdot H_2O_2$ (3:1 volume%) mixture solution and sputtering Cr (500 nm)/Au (1800 nm) metal films; (2) Coating photoresist S1808 and patterning the resist for basic sensor structure; (3) Wet etching Au/Cr metal films and removing the resist; (4) Coating lift-off resist LOL2000 and photoresist S1808

and creating lift-off pattern by two-step development method; (5) Wet etching quartz wafer in saturated bifluoride ammonium solution at 87 ^{o}C for 1 hour; (6) Etching the Au/Cr mask metal films, the part of which are not protected by lift-off pattern; (7) Sputtering Cr/Au/Cr (800 nm/3800 nm/3000 nm) metal films; (8) Lifting-off the unwanted metal films using Shipley remover 1161 at 80 ^{o}C for 1 hour; (9) Wet etching Au/Cr metal films protected by the lift-off pattern.

In this process, LOL2000 are coated two layers for increasing the undercut height. The following is the detailed coating sequence. (1) Spin-coating LOL2000 on the front side at 4000 rpm for 30s and prebaking in an oven at 150 ^{o}C for 5 min; (2) After 5 min cooling in air, spin-coating and prebaking LOL2000 on the back side with the same treatment as (1); (3) After 5 min cooling, respin-coating and prebaking LOL2000 on the front side with the same treatment as (1); (4) After 5 min cooling, respin-coating and prebaking LOL2000 in an oven at 150 ^{o}C for 30 min.

After etching quartz substrate, the resist pattern was examined by optical microscope and SEM (scanning electron microscope). Fig. 3.11 (a) shows the leading wire and pad pattern and the black edge is the overhang part. Fig. 3.11 (b) gives the cross section of undercut profile after quartz etching. These results demonstrated that the overhang created by two-step development method was resistive to the aggressive quartz etchant. Fig. 3.12 gives the full view of tilt sensor. The surface wires and pads were clearly patterned and through the SEM picture it can be learnt that the side wall metal films were also protected. The specially designed through holes, which are used for isolating the electrical electrodes, were also patterned. By breaking the side of the though hole, electrodes can be isolated, which were connected by the side wall metal films. The final Cr layer in the tri-layer metal films Cr/Au/Cr is used for protected the Au layer when etching the surface Au metal film in the last step process. And after etching Au, the final Cr layer is also removed when etching the quartz etching mask Cr. Finally, the whole electrode is Au/Cr films. Cr layer is used as adhesive layer, because Au does not adhere to quartz well. Here Au is used as the main electrode and pad metal

because it has low electrical resistivity and it is hard to be oxidized, which benefits to the following packaging process. The thick films in the second deposition are for ensuring the side wall metal films due to step coverage phenomenon. The fabricated tilt sensor was also measured by impedance analyzer for examining the initial capacitances. Considering the parasite capacitance, the measured results which are 3.38 pF at left side and 3.29 pF, agree well with the designing value. The successful fabrication of tilt sensor suggests the effectiveness of the proposed lift-off process.

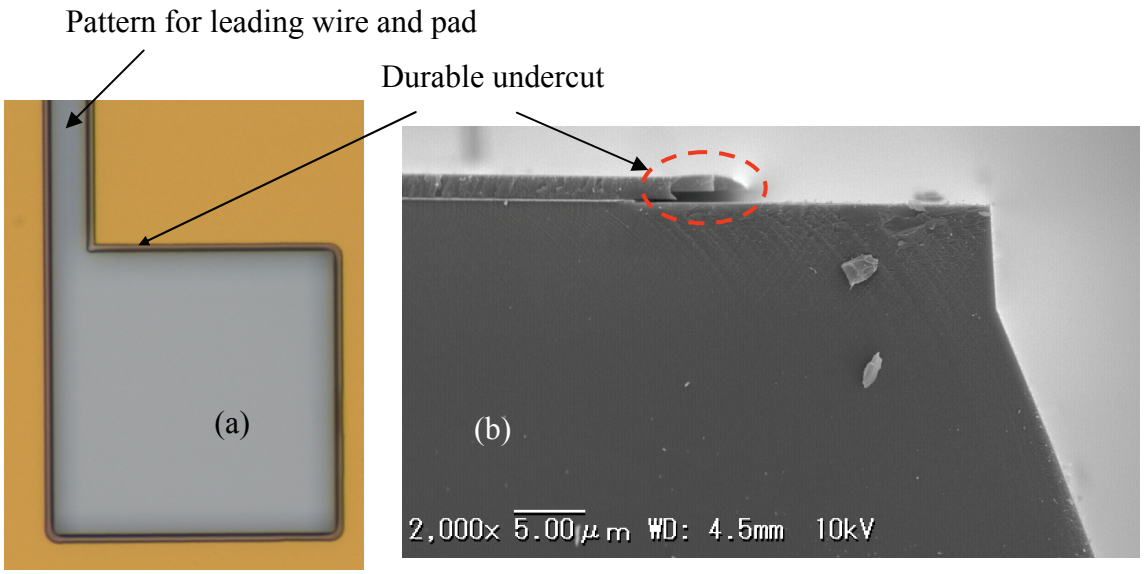


Fig. 3.11. Overhang structure after etching quartz: (a) Top view of undercut profile; ((b) Overhang cross section on etched quartz wafer

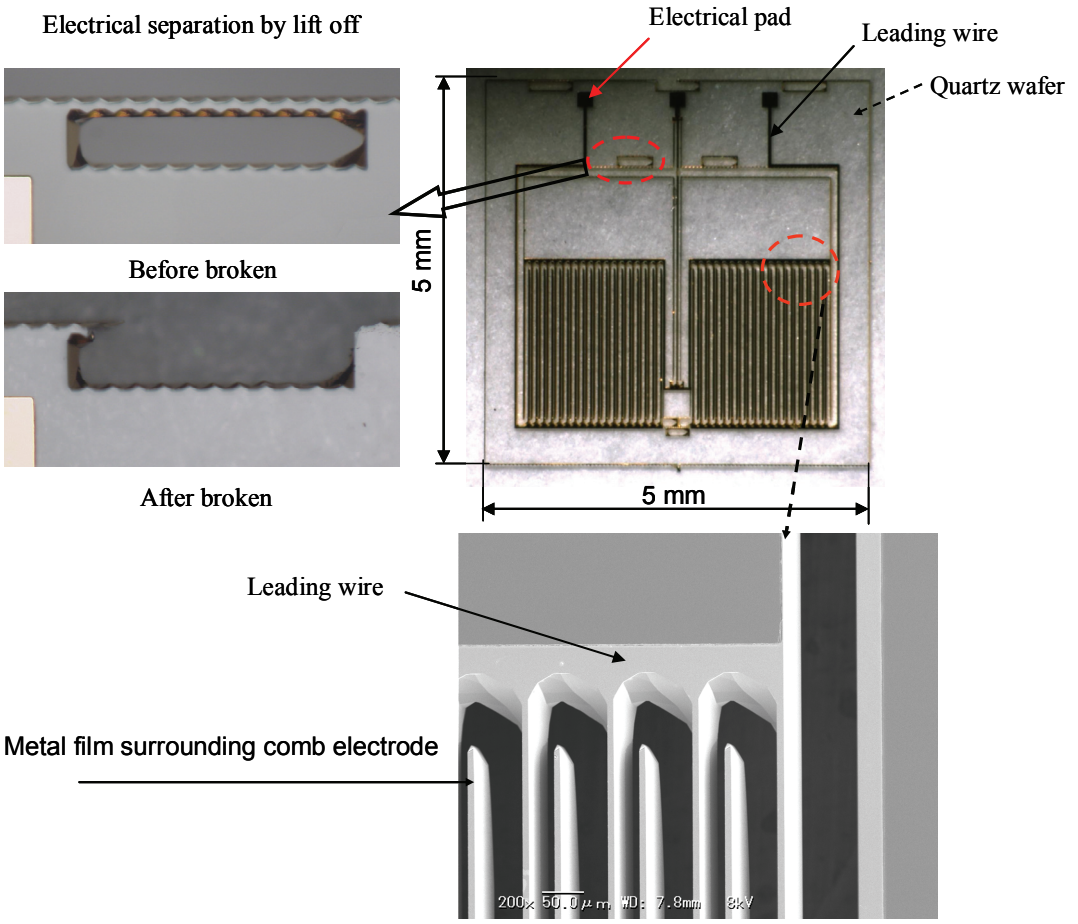


Fig. 3.12. Fabricated tilt sensor

3.3.2. Quartz MEMS resonator

Modern communication systems such as programmable radios and GPS receivers require ultra small, high frequency filters and oscillators with extremely good temporal and thermal stabilities, high resonant quality-factors, and excellent RF matching characteristics. Quartz resonators have been the prevailing choice for such

applications because single crystal quartz has several attractive material properties. It is low loss (high Q) piezoelectric material with zero temperature coefficient for selected crystal cuts. In addition, its chemically inert surface makes quartz a candidate for stable frequency operations [9]. Unfortunately, current quartz resonator manufacture technique, mainly mechanical milling, has a thickness limitation of about several tens μm due to the mechanical strength, which dominates the basic resonation frequency in the case of AT cut. Recent advancements in microfabrication, especially in the areas of precision wafer bonding and plasma etching, have enabled us to fabricate miniaturized quartz on-chip resonators working in the VHF-UHF frequency range [9-11]. However, these processes are expensive and need special equipments.

On the other hand, silicon based MEMS resonators have received significant attention over the past 20 years [13] and have been considered to replace quartz resonators. The main obstacle for the further development of quartz resonator is the insufficiency of quartz microfabrication knowledge.

This research aims to fabricate high frequency MEMS resonator using the cheap bulk wet etching technique. Proposed resonator is shown in Fig. 3.13. The wafer is AT cut single crystal quartz. It consists of vibration part, leg and holding part. Resonator part is etched to the desired thickness for getting wanted frequency, for example, for

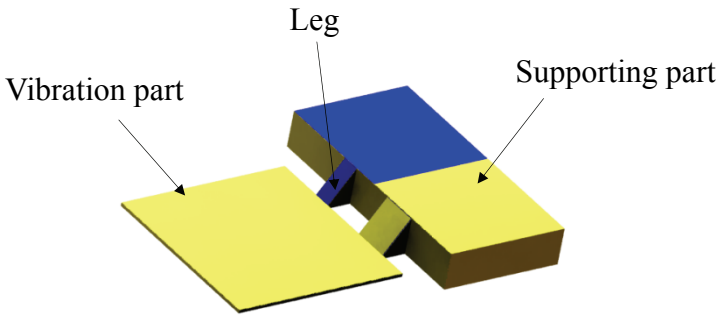


Fig. 3.13. Schematic diagram of high frequency resonator

getting 622 MHz resonator the thickness should be 2.2 μm. The holding part is for mechanically and electrically bonding the resonator. And legs are for separating the vibrating part and holding part.To fabricate such a resonator, in general consideration, the process should be designed as Fig. 3.14. (1) Washing AT quartz wafer using Piraha solution; (2) Sputtering Cr/Au metal films as quartz etching mask; (3) Spin-coating and patterning photoresist (softbaking, exposing to UV light, developing and hardbaking); (4) Etching Au/Cr metal films and removing photoresist; (5) Etching quartz; (6) Etching Au/Cr metal films; (7) Sputtering Cr/Au metal films; (8) Coating and patterning

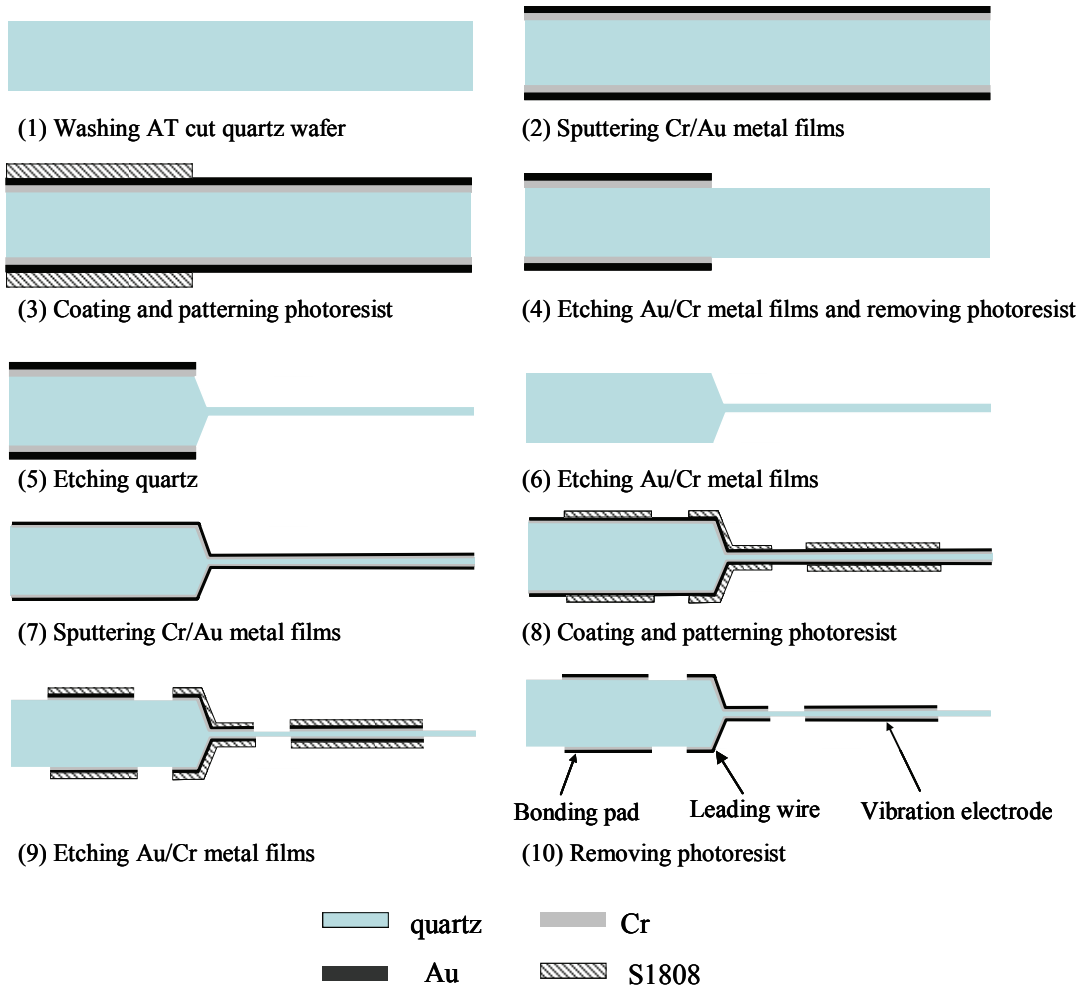


Fig. 3.14. Traditional process flow for fabricating resonator

photoresist; (9) Etching Au/Cr; (10) Removing photoresist. In this process, resist should be coated on the different level surface and tapered sidewall and patterned. In reality, it is difficult to do these due to the complex sidewall profile, especially in the case of minus angle of side wall, which may appear when etching AT cut quartz [14-16]. For achieving these goals, special resist coating equipment and exposure equipment are needed.

Using the developed lift-off method, fabrication process of MEMS quartz

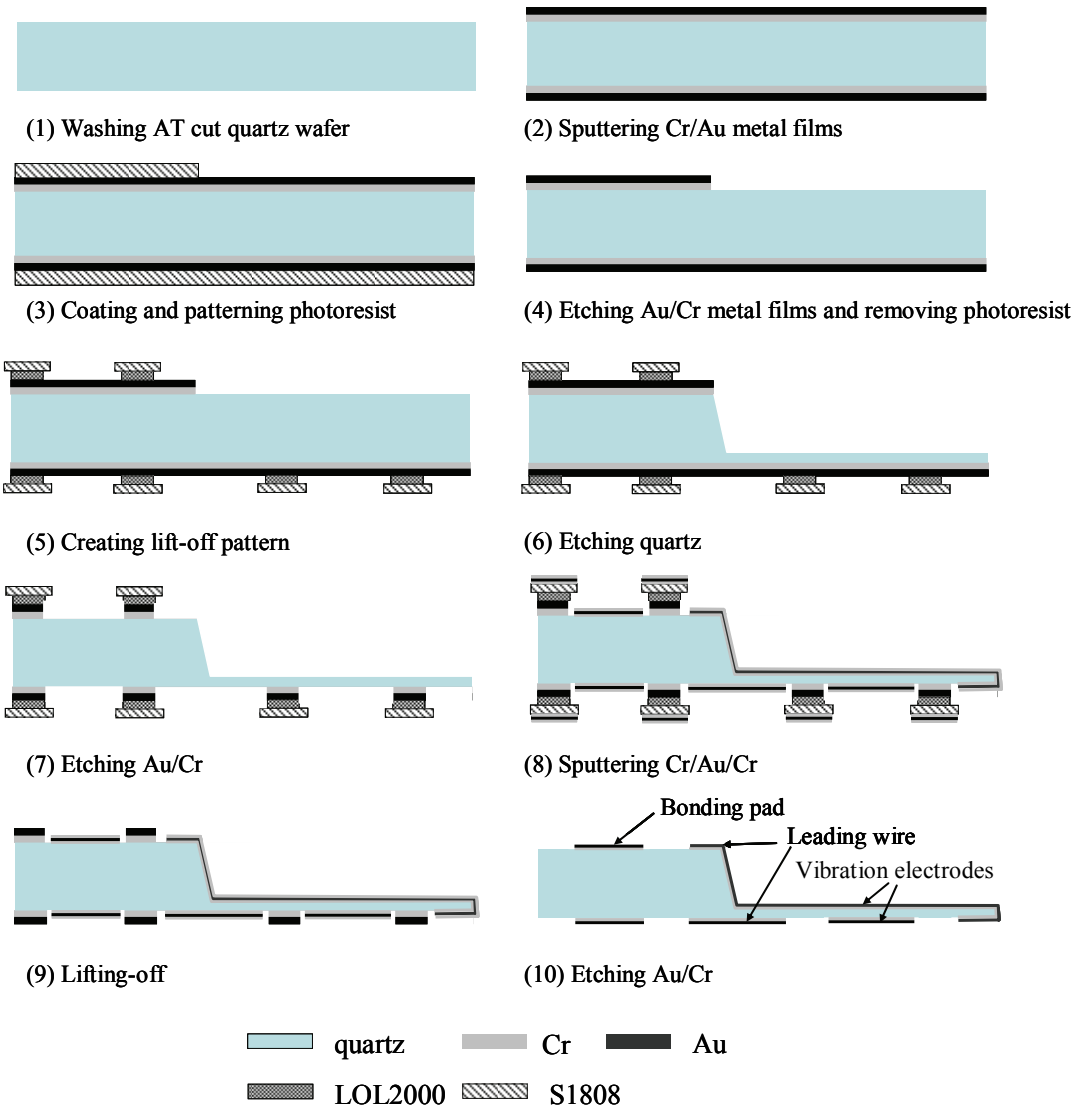
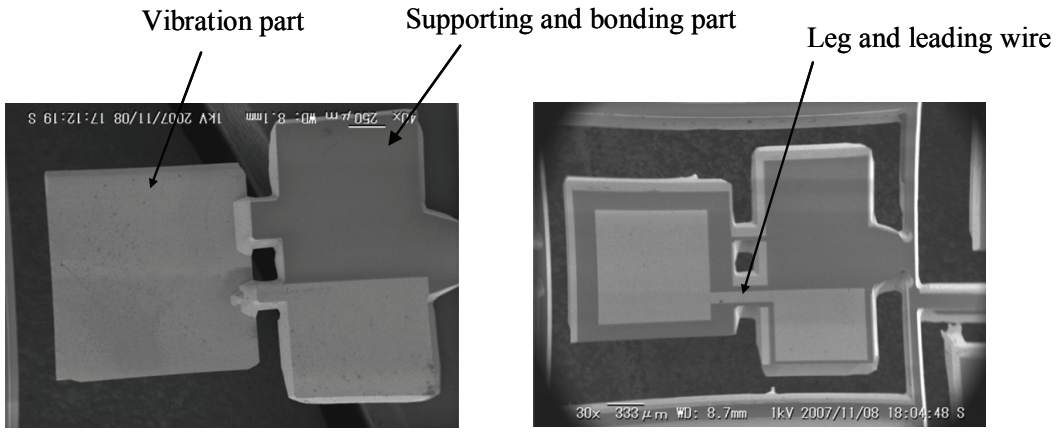


Fig. 3.15. Lift-off process for fabricating MEMS quartz resonator

resonator can be designed as Fig. 3.15. (1) Washing AT cut quartz wafer; (2) Sputtering Cr/Au metal films; (3) Spin-coating and patterning photoresist S1808 on the double sides; (4) Etching Au/Cr; (5) Creating lift-off pattern for the final metal electrode; (6) Etching quartz; (7) Etching Au/Cr metal films; (8) Sputtering Cr/Au/Cr metal films; (9) Lifting-off; (10) Etching Au/Cr.

Fig. 3.16 shows an example of fabricated MEMS quartz resonator. The thin vibration part can be seen from Fig. 3.16(a) and the electrodes' separation can be learnt from Fig. 3.16 (b). Detailed information about the fabrication condition and evaluation



(a) Front view (b) Back view

Fig. 3. 16. SEM pictures of fabricated quartz MEMS resonator: (a) front view; (b) back view

results of the resonator can be found in [16].

3.3.3. Electrical interconnection

With the development of integration, multilayer mounting or wafer level packaging has become a hot topic. Proposed lift-off process can also contribute to this goal, because no resist is needed to coat on the high aspect ratio via or through-hole side walls. Fox example, for packaging the MEMS resonator mentioned above, two bonding

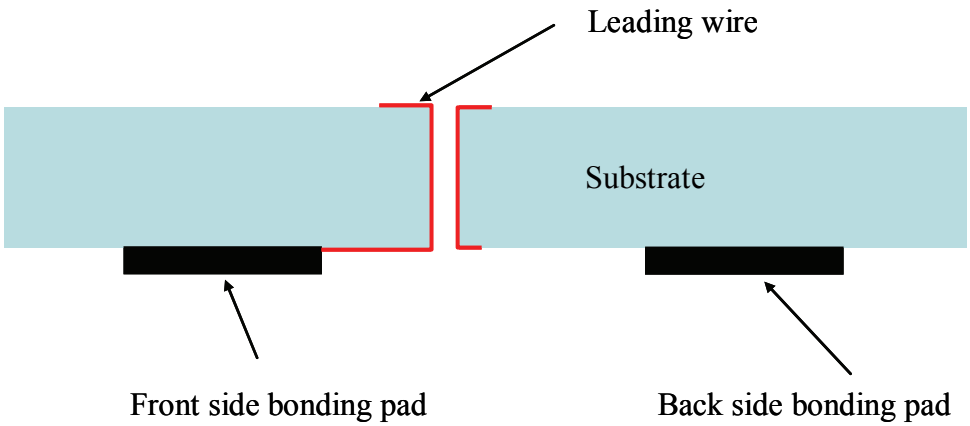


Fig. 3. 17. Schematic diagram for interconnection

method should be used, wire bonding for the front side and flip chip bonding for the back side. Wire bonding would increase the space and wire length. Further, our group research has demonstrated when wire bonding the front side pad after flip chip bonding the back side pad, the metal films can be easily peeled off. Detailed flip chip packaging knowledge would be introduced in chapter 5. Using the lift-off process, we can lead the front side electrical pad to the back side as Fig. 3.17. Then the two side pads can be bonded at the same time using flip chip technique, and the wire bonding process can be deleted.

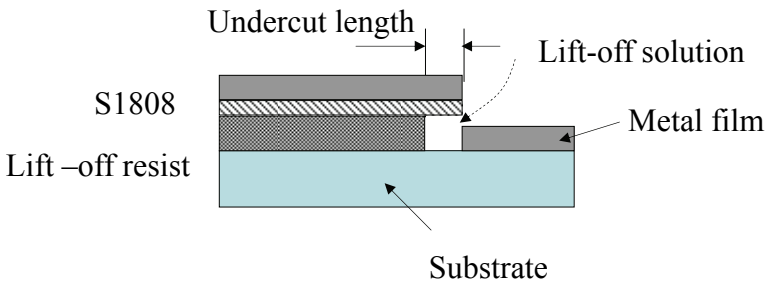


Fig. 3.18. Schematic diagram of undercut profile

3.4. Summary and discussions

A bi-layer lift-off process using lift-off resist LOL2000 for 3-D patterning was built up. The main differences with the conventional planar lift-off process are that the lift-off is created before etching substrate and the overhang structure should also compatible with the step coverage requirement of MEMS devices. A two-step development was demonstrated effective to create such a strong overhang. Quartz MEMS based capacitive tilt sensor and resonator were successfully fabricated using the proposed process.

LOL is a thin resist which is designed for lifting-off thin metal. For clean lift-off processing, the lift-off resist layer should be thicker than the deposited metal thickness, typically 1.2-1.3 times the thickness of the metal film for introducing lift-off solution (Fig. 3.18). In the 3-D patterning application, usually thick metal films are needed due to the step coverage phenomenon. That means multi-layer LOL resist should be coated for increasing the lift-off resist thickness. Multi-layer coating will result in bad uniformity. However, recently a thick lift-off resist LOR has been supplied by the Microchem Corp. Fig. 3.19 gives the thickness data sheet (from both product data sheets) of resist Shipley LOL and Microchem LOR. For extensive applications, we would investigate the LOR performance for the 3-D lift-off process.

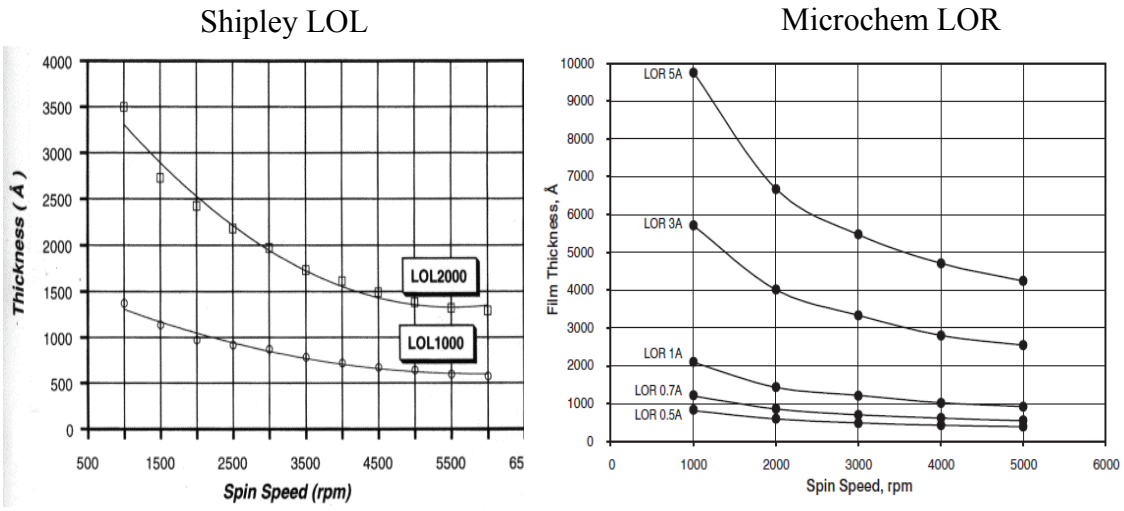


Fig. 3.19. Thickness data sheet of lift-off resist LOL and LOR

3.5. Improvement of lift-off process using LOR resist

Based on the same idea as the LOL lift-off process, the thick lift-off resist is investigated and confirmed for fine pattern fabrication on quartz substrate [15-16].

3.5.1. Optimization of undercut profile

Undercut profile was created using the two-step development method built up in the LOL process. The coating and baking conditions and development conditions are also the same as the LOL process. The lift-off resist used here is LOR15A (1.5 μm thick). Here, the dependence of the undercut length on development time is

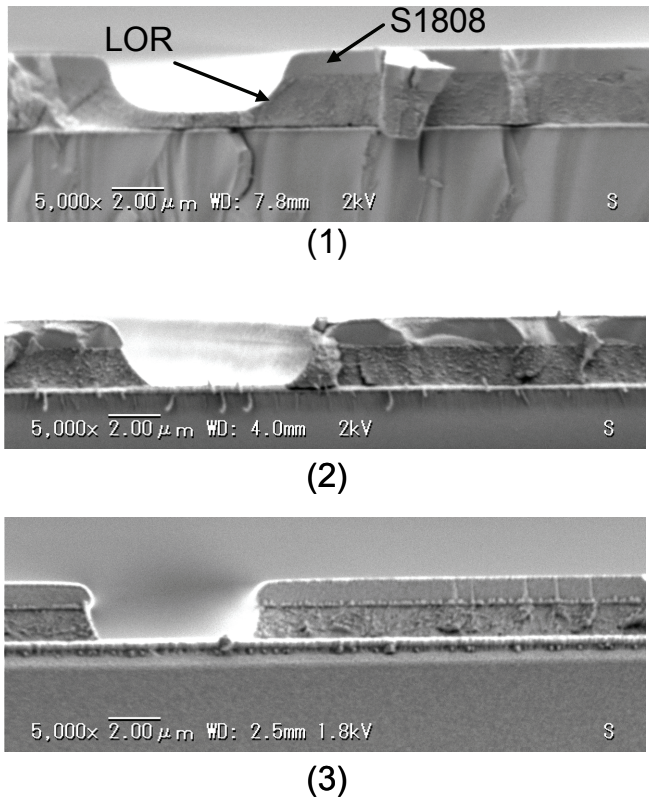


Fig. 3. 20. SEM pictures of undercut profile after the first step development: (1) 30 s; (2) 45 s; (3) 60 s

investigated.

According to the results (Fig. 3.20), 60 s was selected as the first step development time. Following 30 min hard-bake at 150 ^{o}C in an oven, the second step development was performed from 80 s to 120 s respectively. Fig. 3.21 shows the development results. High aspect ratio undercut (AR=undercut length: lift-off resist thickness) was achieved in this step. No dropping off was observed even large overhang as 1.8 μm at 120 s development. This result should be contributed by the hard-baking treatment. Generally, the larger overhang, the easier lift-off because a high aspect ratio undercut can avoid continuous metal films on and under the resist. Selection of development time (undercut length) should also depend on the aspect ratio of the substrate microstructure to be

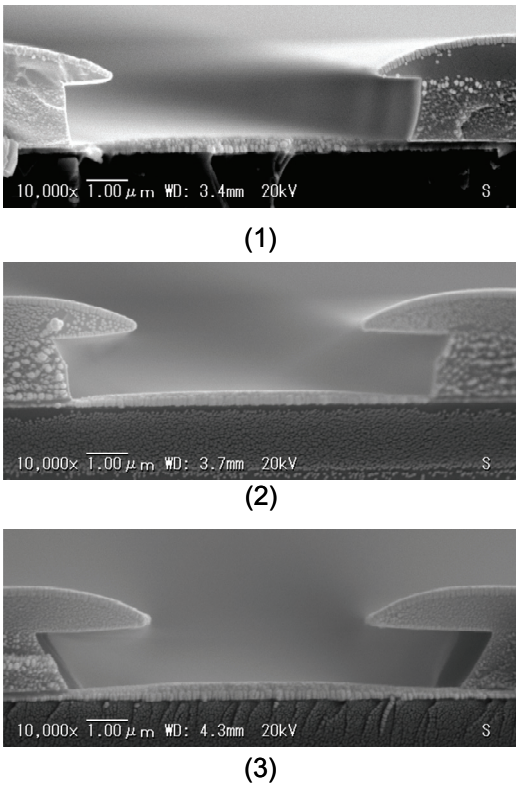


Fig. 3.21. SEM pictures of undercut profile after the second step development: (1) 80 s; (2) 100 s; (3) 120 s

coated.

3.5.2. Patterning 3-D microstructure

High aspect ratio microstructure was fabricated by anisotropic etching Z cut quartz wafer at polar angle 45°. The fabrication of high aspect ratio microstructure on quartz was referred to our publication and chapter 2. Saturated ammonium bifluoride solution at 87 ^{o}C, which is commonly used for etching quartz with an etching rate of 110 μm/h at Z direction, was used as quartz etchant. The surface pattern was defined as 5 μm/5 μm,

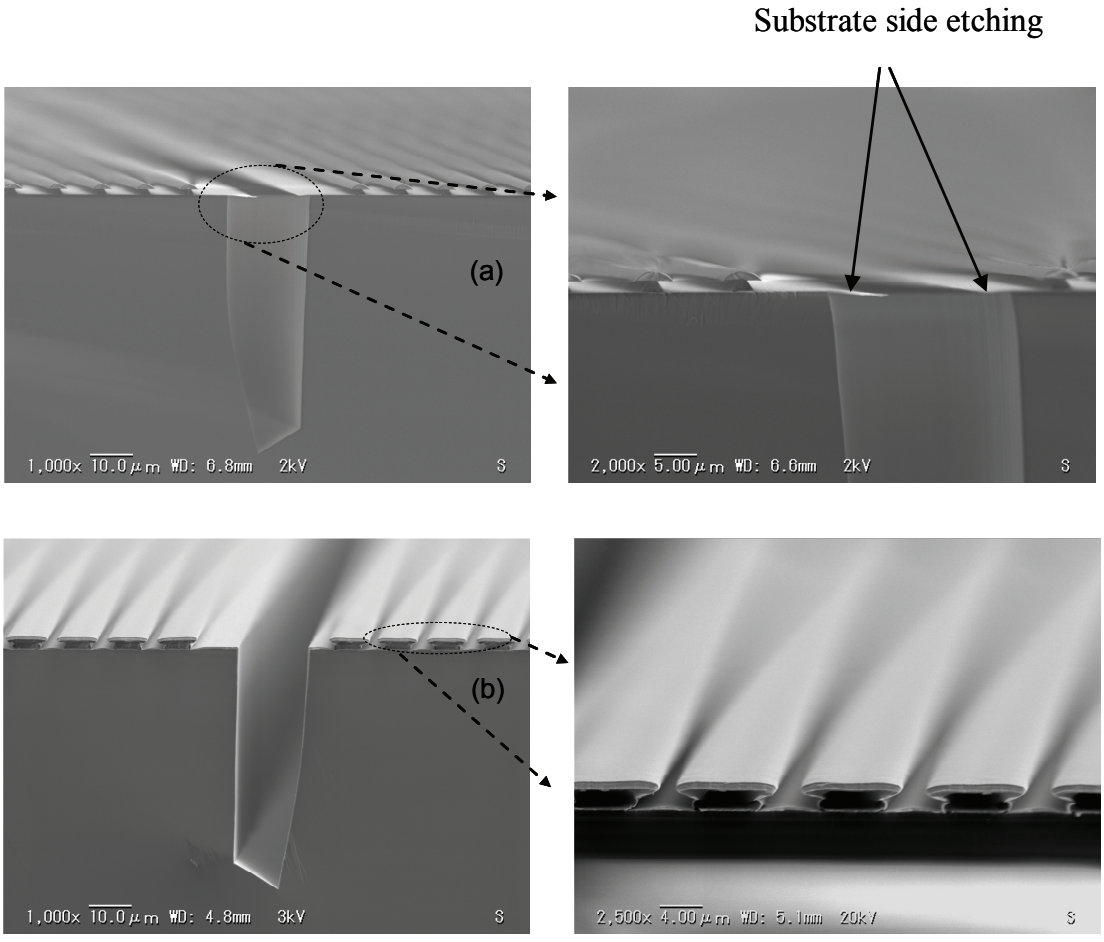


Fig. 3.22. Lift-off pattern on 3-D microstructure: (a) after etching quartz; (b) after sputtering metal films

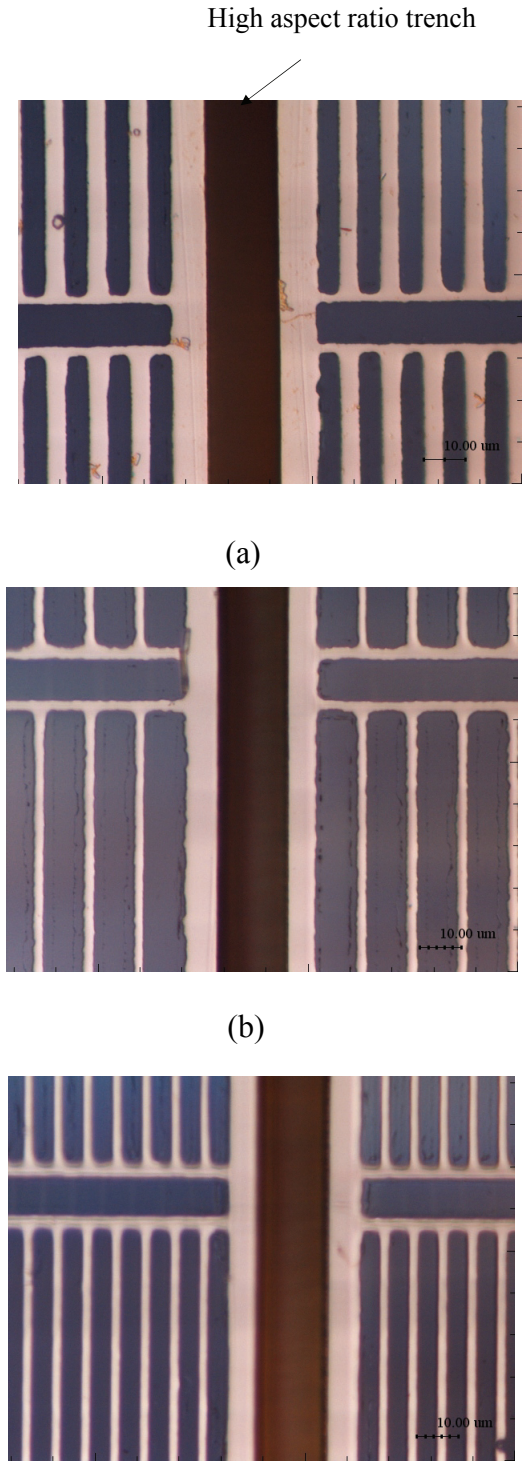


Fig. 3.23. Fabricated fine line/space pattern on high aspect ratio microstructure: (a) L/S=5 um/5 um; (b) L/S=2 um/10 um; (c) L/S=2 um/5 um

2 μm/10 μm and 2 μm/5 μm at line/space, respectively. And the opening space for etching substrate was 5 μm. Corresponding to the process flow in Fig. 3.3, sputtered Cr/Au films were used as Film A, and Cr/Au/Cr films were used as Film B. Lift-off was performed in the Microchem remover PG solution at 60 ^{o}C for 1 hour.

Fig. 3.22 (a) shows the cross section of the 60 min etched structure with 5 μm line and 5 μm space pattern. The aspect ratio (depth:/width) of the trench was 2.7. The result demonstrated that optimized overhang structure and the LOR resist withstood the corrosion of aggressive substrate etchant. In this experiment, the second step development was performed at 100 s. Au/Cr metal films, which was used as the substrate etching mask, were etched because these films will affect the next metal deposition on the side wall of the trench. Fig. 3.22 (b) shows the cross section of 2 μm line and 10 μm space pattern after Cr/Au/Cr metal films deposition. Lift-off removed the Cr/Au/Cr films on the resist, followed by etching the Au/Cr films underneath the lift-off resist. Desired Cr/Au films were left on the surface and sidewall of the trench. Fig. 3. 23 gives the results of successfully fabricated three kinds of patterns and the lines and spaces are 5 μm/5 μm in Fig. 23 (a), 2 μm/10 μm in Fig. 23 (b) and 2 μm/5 μm in Fig. 3. 23. (c), respectively. Two μm line and 5 μm space is considered to be the finest pattern which can be achieved in this process because the hard-baking treatment would reduce the pattern resolution and minimum 2-3 μm wide LOR resist is needed to support the upper photoresist. LOR process was also demonstrated to be able to fabricate the quartz MEMS based tilt sensor as the LOL resist.

Appropriate LOR resist should be chosen depending on the aspect ratio of the microstructures in the device and the thickness of metal films. LORs are available in film thickness from 30 nm to 4 μm. However, thick LOR means worse pattern resolution because high aspect ratio undercut is needed for reducing step coverage. Further, for spin coating thick LOR resist, whisk is a notorious problem, especially for square wafers (Fig. 3.24). Special effort should be made in the future. Limited by the sputtering system and actual application, here Cr/Au films were used as metal A and

Cr/Au/Cr films as metal B. Completely different metal A and metal B are more

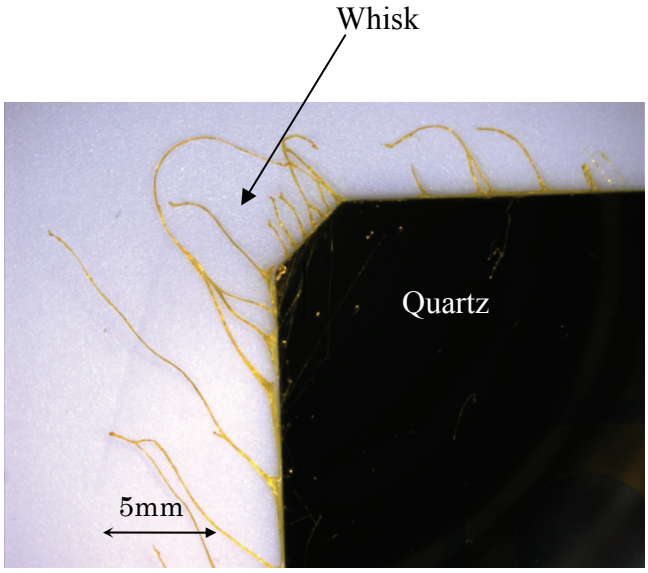


Fig. 3. 24. Whisk of spin-coated LOR15A on quartz wafer

preferable.

3.6. Summary

Lift-off process was improved for patterning 3-D microdevices. The resist pattern for lift-off is created before etching substrate, and the resist pattern should be hard enough to withstand the aggressive substrate etchant. And the undercut should be deep enough to reduce the step coverage which is required by the 3-D microdevice. A two-step development method was developed for creating a high aspect ratio undercut and resistive overhang. The overhang was optimized and controlled by the development time. Both lift-off resist LOL2000 and LOR15A were investigated and demonstrated on this process. Quartz MEMS based tilt sensor was successfully fabricated using proposed process. Further, fine patterns as line/space at 5 μm/5 μm, 2 μm/10 μm in and 2 μm/5 μm on the surface with metal films on the side wall of high aspect ratio trench (AR=2.7) were achieved on quartz wafer. A wide application can be expected in other 3-D MEMS

fabrication.

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Chapter 4 Step coverage improvement by rotation PVD system

4.1. Introduction

Physical vapor deposition (PVD) has long time been one of the techniques of choice for metallization in integrated circuits. In particular, sputter deposition has been widely used in the manufacturing of high-performance on-chip interconnect. When used in the ULSI (ultra large scale integration) and MEMS devices with deep vias and trenches, film deposition through PVD, unfortunately, suffer from shadowing effects if the aspect ratio of the vias and trenches, which is defined as the ratio of the height to width of the structures, is sufficiently large [1]. Several efforts beyond the conventional PVD have been reported for improving step coverage performance. These are long-throw deposition, collimated sputter deposition and oblique angle physical vapor deposition and so on.

4.1.1. Long throw deposition

Geometrically, most conventional PVD systems have short target-to-sample, or throw, distances. This results in the highest deposition rates, as relatively few atoms are lost to the chamber sidewalls. By moving the sample farther away from the target, an increasing fraction of the sputtered atoms, particularly those which are moving mostly laterally are lost to the chamber walls. Further increases in the throw distance result in a greater loss of these non-normal incidence atoms, while the normal-incidence atoms still deposit on the sample. This requires, of course, that the operating chamber pressure be low enough that the mean free path for the sputtered atoms exceeds the throw distance [2-4]. Long throw is a simple directional deposition method.

However, low-throw deposition applications are strongly limited by a fundamental geometrical asymmetry problem [2, 5]. In the case of sample positions on the centerline of the chamber, the angular distribution of the arriving flux is symmetric about the surface normal. However, as the edge of the sample wafer is reached, the deposition

becomes nonsymmetrical due to the relatively larger area of the target to the center of the system compared to the edge. The typical level of the asymmetry is about 2-3 times, meaning that the thickness of the deposited film on the inward-facing sidewall is two to three times the thickness on the outward-facing sidewall [2]. This ratio is dependent on the trench aspect ratio (see Fig. 4.1). In short, the technology does not scale well to larger samples.

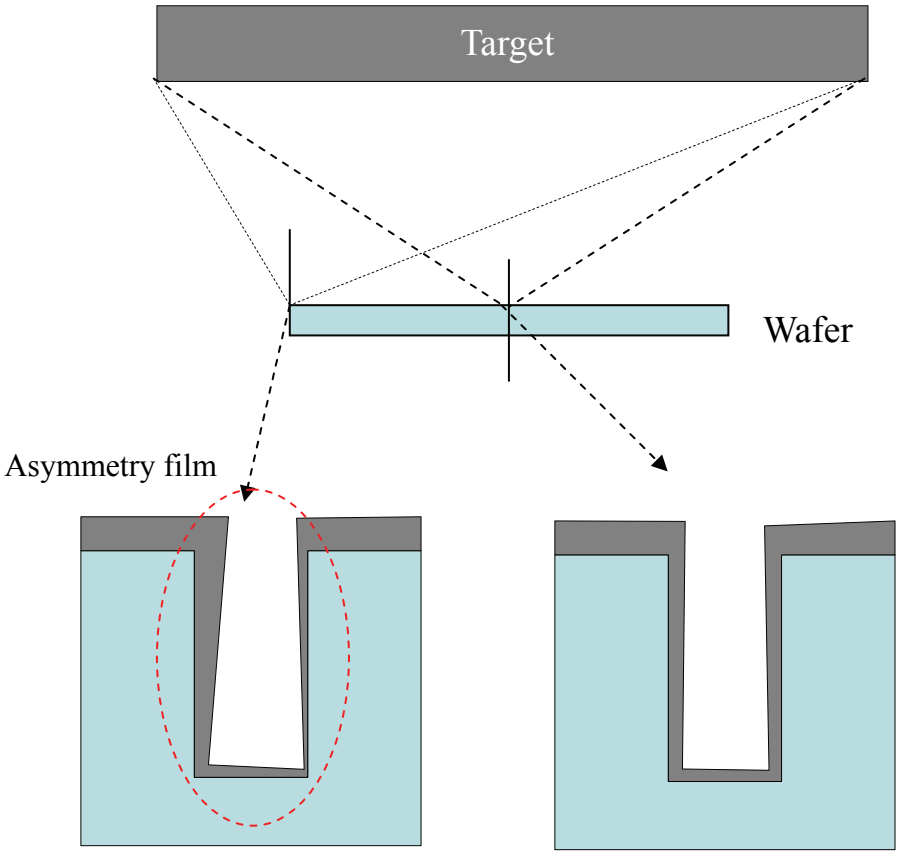

Fig. 4.1. Asymmetry depositing flux at the wafer edge

4.1.2. Collimated sputter deposition

Fig. 4.2 shows a schematic diagram of collimated sputter deposition system. The collimator serves as a directional filter by simply collecting the atoms which impinges

on its walls. The degree of angular filtering is related directly to the aspect ratio (length to width) of the collimator cell as well as to the physical location of the collimator [2].

There are several problem associated with collimated sputtering. These include particle generation and the build-up of sputtered material on the collimator, which necessitates frequent replacement of the collimator. Collimation also affects film properties, particularly stress. Another major issue with collimated sputtering is its efficiency. Since only the atoms within a certain range of angles can pass through the collimator. Only a fraction of the sputtered atoms actually end up on the wafer. The rest are deposited on the collimator, and are therefore wasted, same as the long throw deposition technique [6].

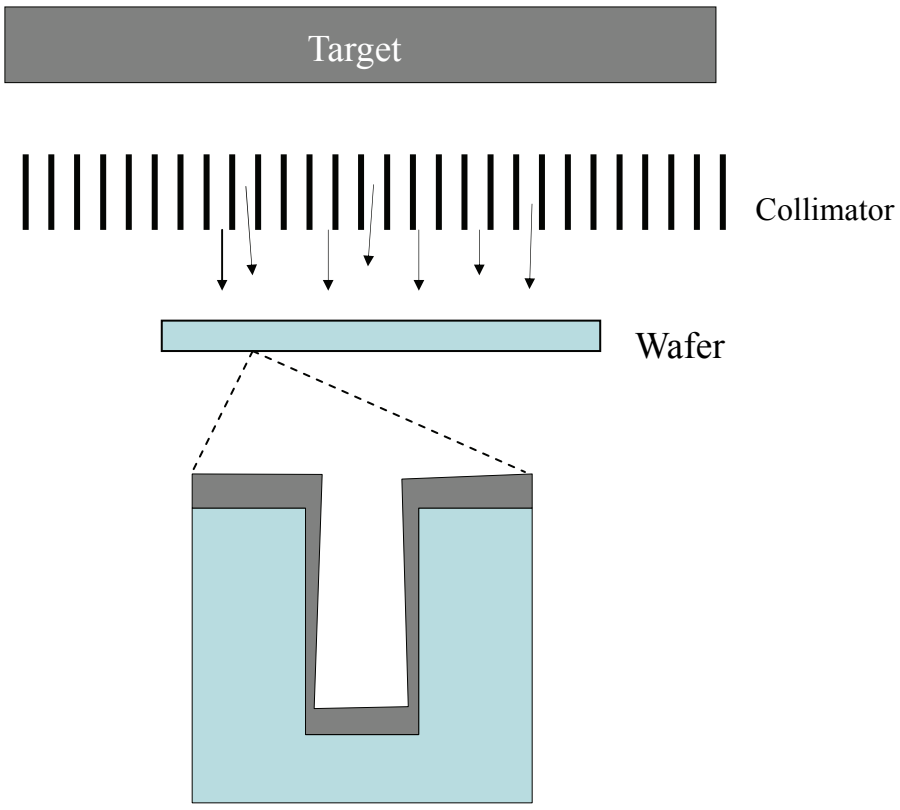

Fig. 4.2. Schematic of collimator based PVD system

4.1.3. Oblique angle physical vapor deposition

OAPVD (Oblique angle physical vapor deposition) system simply combines a conventional PVD system with a tilted angle (with respect to the substrate surface normal) while rotating the substrate [1]. The substrate tilt angle is chosen such that the particles obliquely incident on the patterned substrate can reach more uniformly to the side walls and bottom corners of the trenches/vias avoiding the shadowing effect.

Compared to the directional deposition (long throw and collimated sputtering), OAPVD contributes more on the step coverage on the side wall, which is interesting to MEMS concerns. However, this method has the same drawback as the long-throw deposition method, which is the asymmetry problem on the wafer edge. This is because the rotation does not change the wafer position to the target.

4.1.4. Proposed sputtering system

Proposed sputtering system is shown in Fig. 4.3, a modified sputtering machine SPP-430H. Similar to OAPVD system, the wafer is rotated to make the target incident atoms at all angles possible. The side wall step coverage improvement can be expected. Further, the wafer revolves around the chamber reducing the asymmetry problem on the wafer edge. The distance between target and wafer is 150 mm, which can be relatively considered as long-throw compared to conventional PVD (40-50 mm). On the revolution orbit, for the quartz wafer (39.5mm×41.5 mm), five wafer holders can be set. And one holder can set up three pieces of wafers. The rotation at all 360° specially benefits to the side wall coating of through holes.

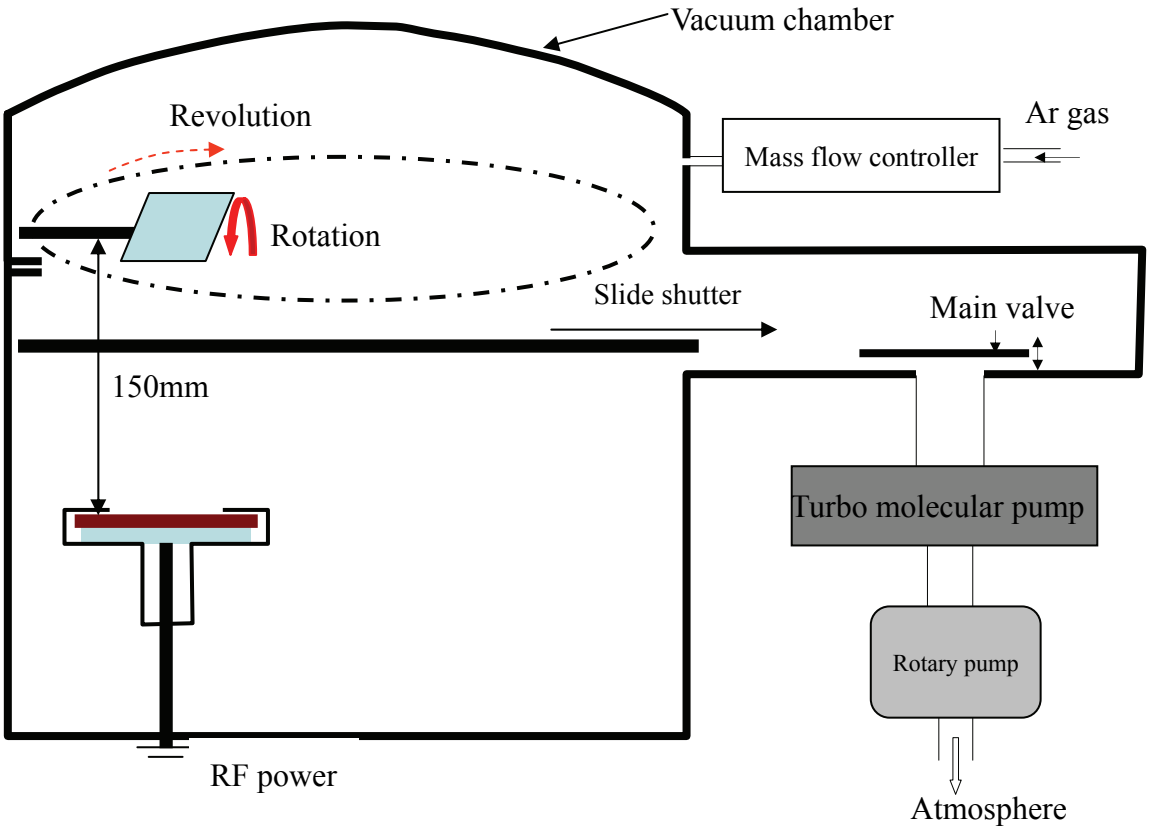

Fig. 4.3. Basic SPP-430H sputtering configuration

4.2. Experimental

4.2.1. Preparation of high aspect ratio microstructure

For examining the effectiveness of proposed sputtering system, high aspect ratio microstructure was prepared using standard quartz etching process, introduced previous (in chapter 1). (1) Washing 100 μm thick Z cut quartz wafer using Piraha solution at 110 degree Celsius; (2) Double-sided sputtering Cr(500 nm)/Au (1800 nm) metal films; (3)Spin-coating photoresist S1808 and softbaking at 90 degree Celsius for 15 min in an

oven; (4) Double-sided exposing the wafer and developing; (5) Hardbaking the wafer at 120 degree Celsius; (6) Wet etching Au/Cr metal films using respective etchant; (7) Removing resist using Shipley remover 1161 at 80 degree Celsius; (8) Etching quartz using saturated bifluoride ammonium solution at 87 degree Celsius for 1 hour; (9) Etching Au/Cr metal films.

4.2.2. Sputtering Cr metal film

In this experiment, 300 nm Cr metal film was sputtered on the surface for lowering the cost. Fig. 4.4 gives the image of sputtering system.

4.3. Results

After sputtering, the sample was cut vertical to the pattern direction. Fig. 4.5 gives the cross section of the microstructures. The opening width is 30 μm and the wafer thickness is 100 μm, with an aspect ratio of 3.3. The metal thickness was examined by high magnification pictures. And the result is given in Fig. 4.6. The thinnest part

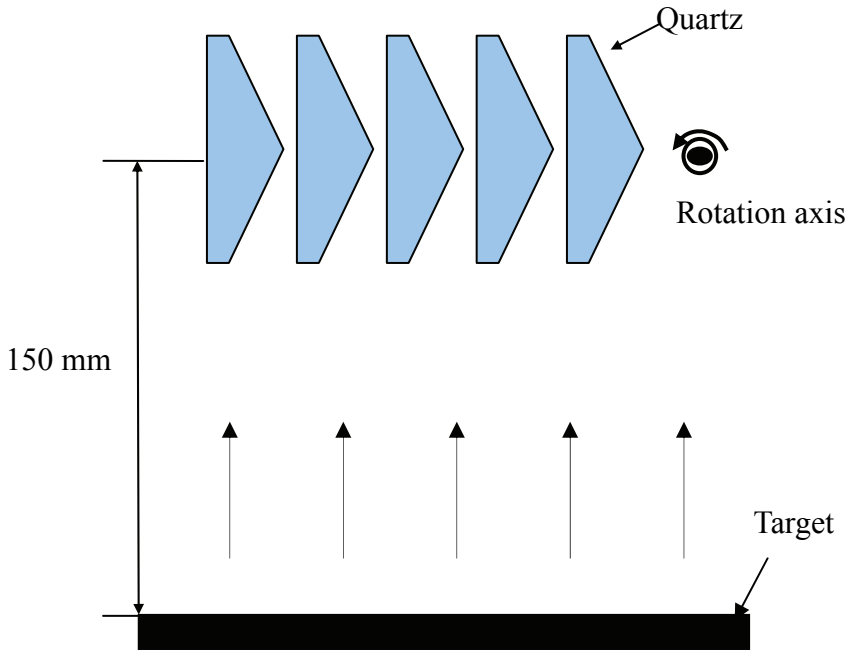

Fig. 4 4. Schematic diagram of sputtering deposition

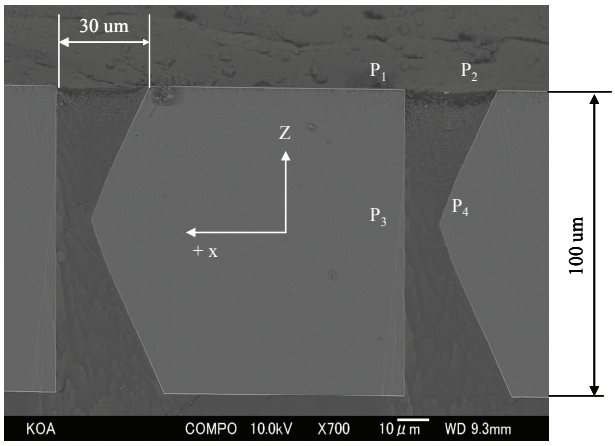

Fig. 4.5. Fabricated high aspect ratio gap on quartz wafer

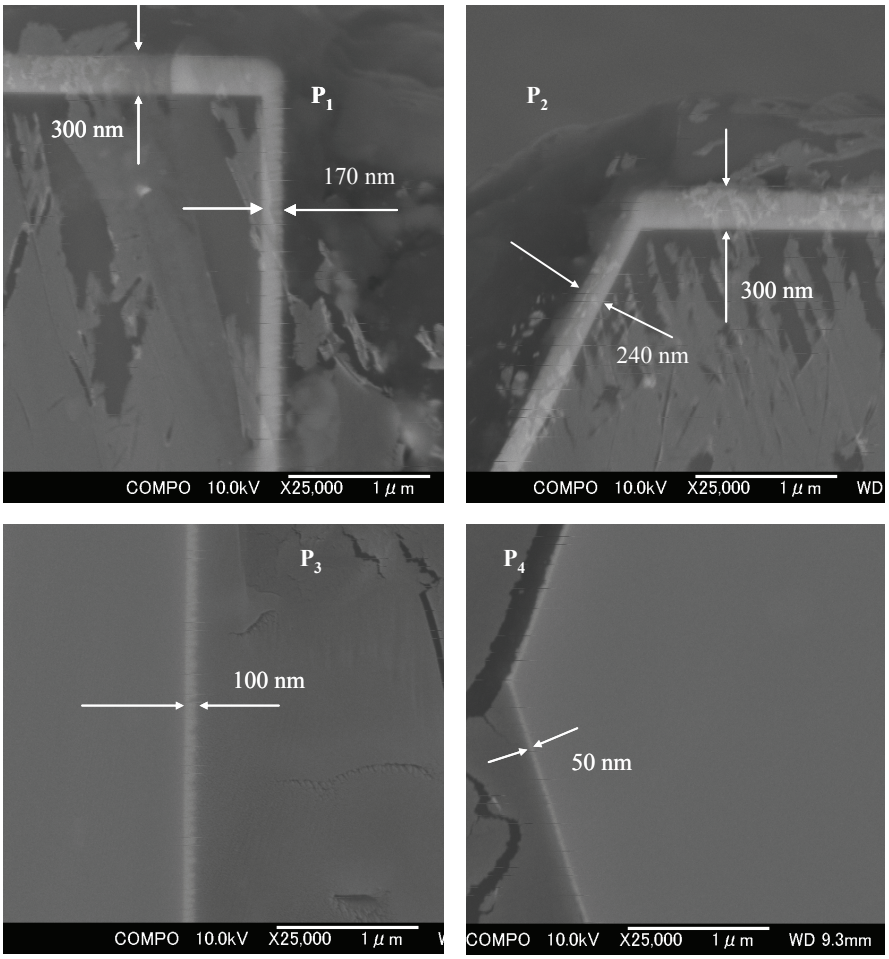

Fig. 4.6. SEM pictures of the high aspect ratio gap and observed step coverage

appeared at the center of tapered side wall, but not the vertical wall. It is considered to be the reason of rotation. The vertical wall center can accept Cr atoms from both sides and the tapered wall center can only receive atoms from single side.

4.4. Discussion and future work

In IC manufacturing, step coverage is usually required for filling trenches or vias with a small opening (μm level). In this case, the bottom step coverage is more important, so the directional deposition is more effective. In the case of MEMS devices, usually conformal thickness electrode is required, so the side wall step coverage is more preferable. For this means, the wafer rotation system seems like a useful way. Although there are also many other ways, such as post-reflow, heated deposition, bias deposition, and those treatments would make the MEMS fabrication process more complex, because these treatments must be compatible with the subsequent processes. For example, in the lift-off process introduced in chapter 3, high temperature should be avoided because it would destroy the lift-off resist pattern.

4.4.1. Optimization of sputtering conditions

Proposed wafer rotation and revolution system has been demonstrated effective for improving side wall step coverage and has been successfully used for fabricating capacitive tilt sensor. However the step coverage should be also dependent on the process conditions, such as sputtering power, working gas pressure, rotation and revolution rate and so on. The next step work is to optimize these parameters.

4.4.2. Residual stress in metal films

There are mainly two kinds of residual stress in metal films. These are thermal residual stress, which is caused by the different CTE between metals and substrate, and internal stress. Internal stress is more complex. Generally, in the case of double-sided metal coating system, when same films are coated on the two sides, the effect of residual stress can be neglected. However, in some cases, the residual stress should be counted in. For example, the deflection of comb electrodes in tilt sensor mentioned in

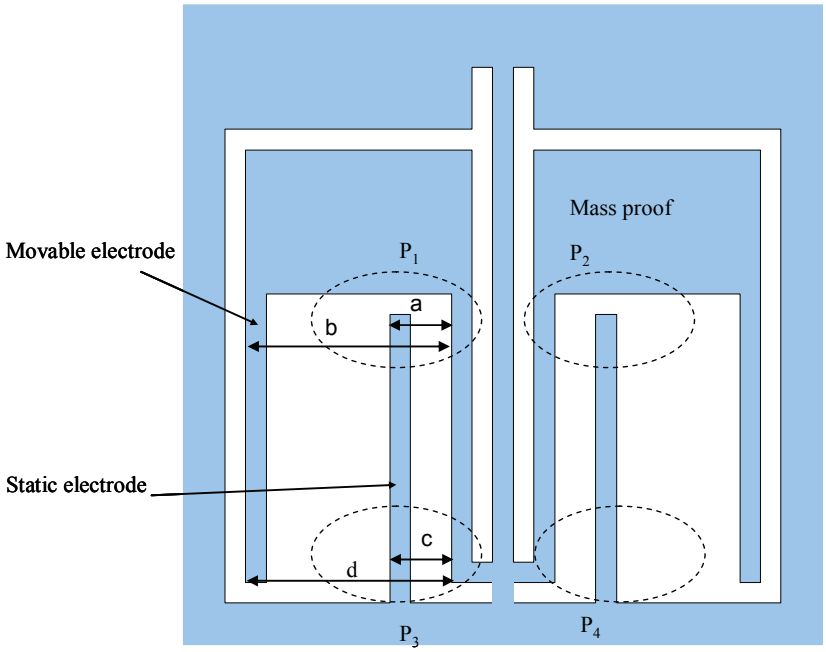

Fig. 4.7. Schematic diagram of tilt sensor and definition of observing positions and measurement method

Chapter 2 has been observed. Fig. 4.7 gives the schematic diagram of tilt sensor and defines observing positions and measuring method. Because the mass proof part is wide enough, it is considered not deflective. So here the difference of a and c is defined as the deflection of static electrode caused by residual stress. And the difference of b and d is the deflection of movable electrode. Fig. 4.8. gives an example of observed electrode deflection. The unbalance between left side and right side can be clearly observed.

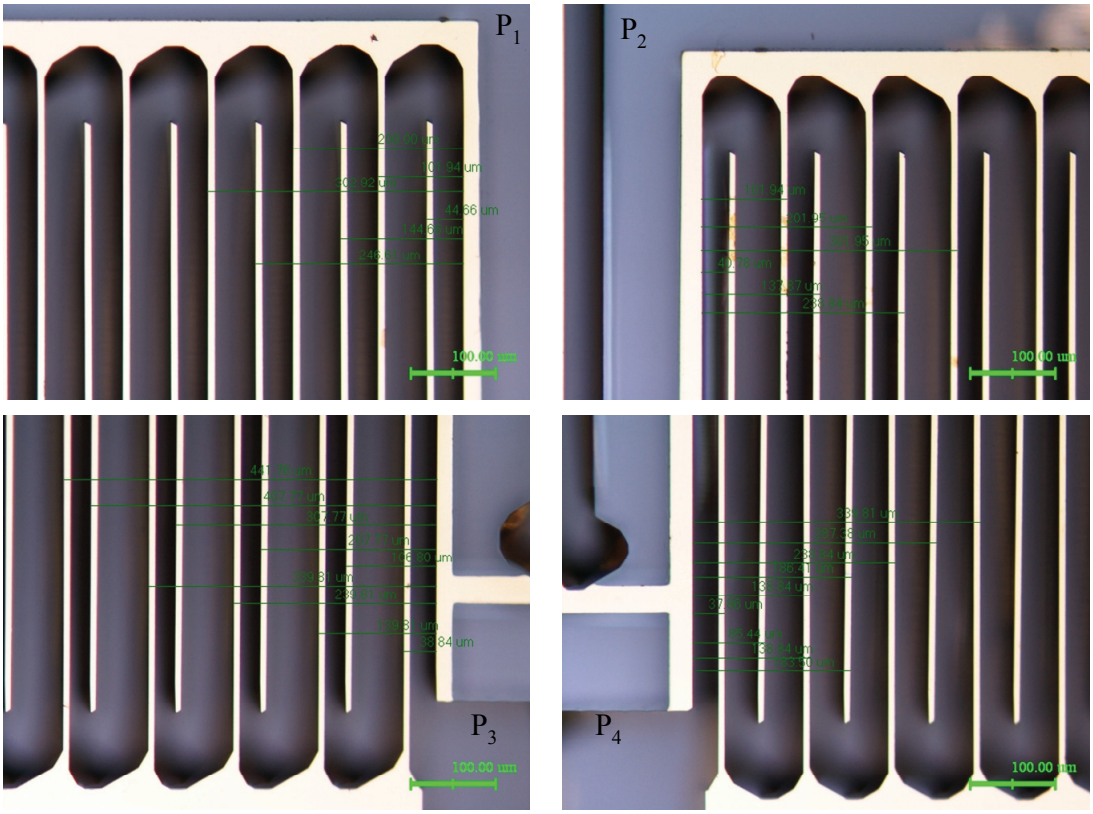

Fig. 4.8. Observed deflection of comb electrodes

Three pairs of comb electrode were measured. Tab. 4.1. shows the average values.

Tab. 4.1. Deflection of comb electrodes

Deflection	Left side (μm)	Right side (μm)
a-c	5.83	-16.5
b-d	-5.82	-0.48

These defections would change the gap between movable and static electrodes

and affects the sensing performance. Annealing treatment is a well known way to reduce the residual stress [7]. Annealing experiment was performed in nitrogen environment for reducing the oxidation of Cr film. The annealing condition was 250 ^{o}C for 4 hours. Fig. 4.9. shows the pictures of annealing treatment results. And Tab. 4.2 summarizes the deflection values after annealing treatment.

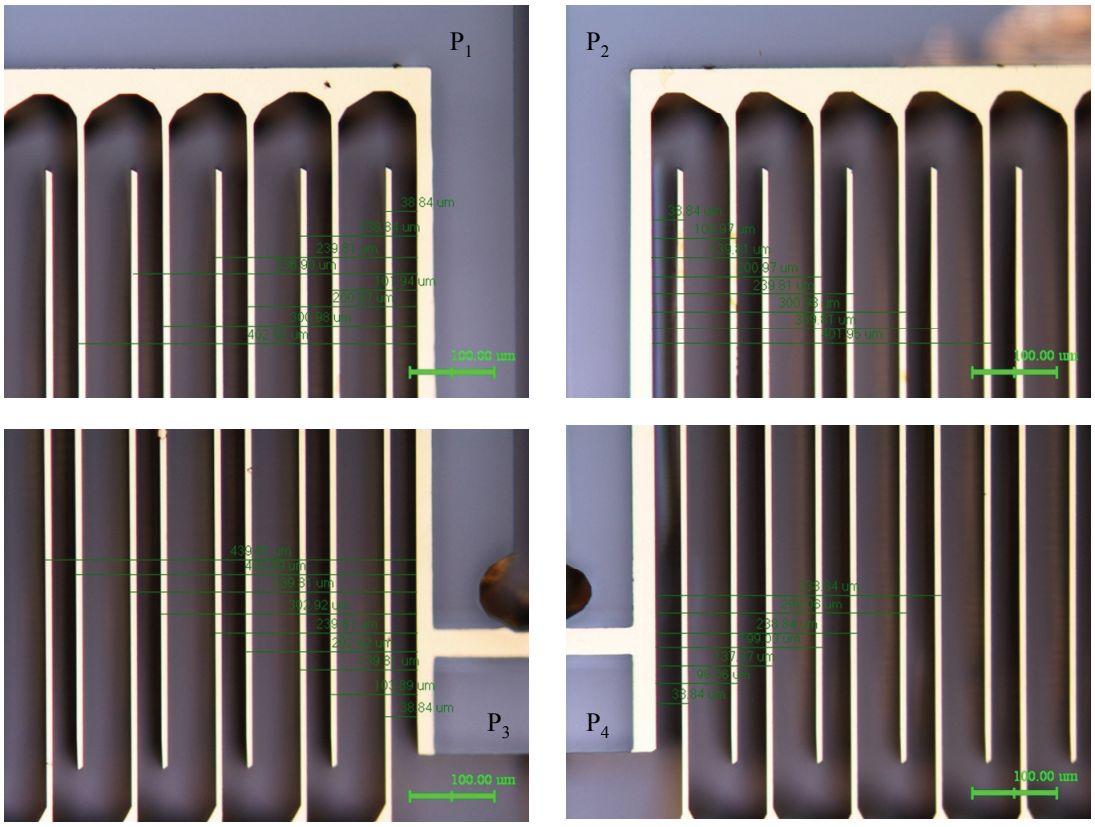

Fig. 4.9. Annealing treated comb electrodes

Tab. 4.2. Deflection values after annealing treatment

Deflection	Left side (μm)	Right side (μm)
a-c	1.95	-2.59
b-d	0.32	-0.97

Compared to the as deposited values, deflection of comb electrodes was clearly modified. However it is difficult to get real balanced between left side and right side, although additional annealing experiments at different conditions were added. Further, it is reported that annealing treatment would promote the diffusion of Cr to Au layer, increasing the electrical resistivity [8-10].

The reason of the deflection is considered to be the different side wall shape and different aspect ratio through holes between the two sides of the comb electrodes. It is very important to control the electrode deflection, since the air gap may need to be manipulated from μm to sub-μm levels.

On the other hand, the residual stress is greatly dependent on the sputtering condition. So, future work would focus on finding the optimum sputtering conditions not only for good step coverage but also for low residual stress.

4.5. Summary

Several step coverage improvement methods were summarized and compared. For improving the side wall step coverage, a wafer rotation and revolution system was proposed. A 100 μm thick and 30 width through hole with tapered and vertical side walls on quartz wafer was prepared for examining the proposed system. According to the surface 300 nm thickness, the thinnest film appeared at the tapered side wall center with a thickness of 50 nm. The deposition system was successfully used for fabricating capacitive tilt sensor. Better step coverage and low residual stress caused by step coverage can be expected by optimizing the process parameters in the future work.

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Chapter 5 Stress free flip chip packaging technique

5.1. Introduction

5.1.1. Flip chip

Flip chip is a bonding technique which provides the electrical and mechanical connection between IC and substrate pad. The solder joint also serves as a path for dissipation of the heat generated by the IC [1]. Instead of wire bonding, flip chip has been gaining acceptance recently, due to the higher number of input/output terminals that can be attached to a given area. The flip chip configuration, a cross section of which is shown in Fig. 1, is such an approach. The IC is turned 'upside down', hence flip chip, and mounted on an appropriate substrate.

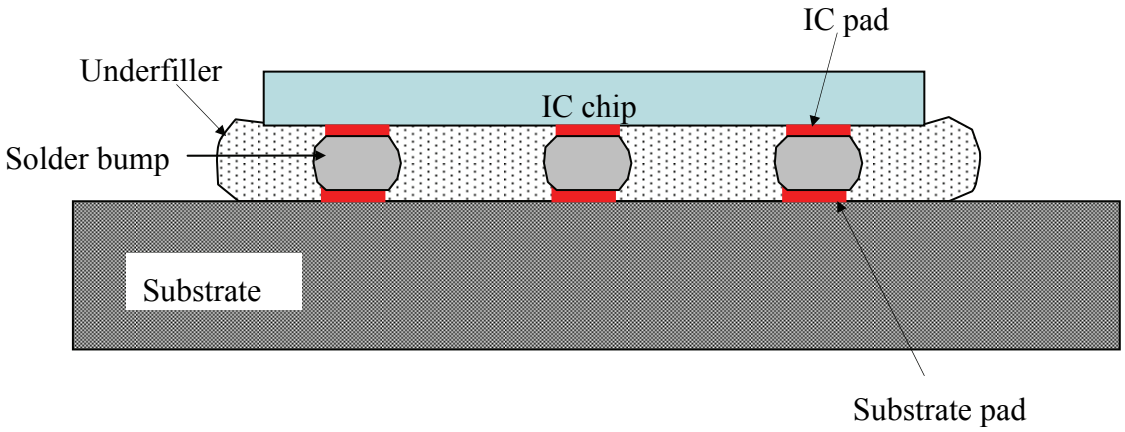

Fig. 5.1 .Cross-section of an IC flip chip connection

Thermal residual stress caused by the large coefficient of thermal expansion (CTE) mismatch between IC chip and substrate is a notorious problem when solder bump based flip chip is applied. In some case of large chip, the warpage of IC chip or substrate caused by residual stress has been reported. Underfilling method is the common way for reducing residual stress in flip chip packaging (Fig. 5.1). The

underfiller works likes the following ways:

- Distribute the residual stress in the IC area
- Enhance the mechanical connection strength between IC chip and substrate
- Prevent the solder joint from oxidation

5.1.2. Concerns for MEMS flip chip

Microelectromechanical systems (MEMS) attract more and more attention in the last decades since 1960s. However, the commercialization of these products is not rapid as expected. One of the most important obstacles is the immature packaging technique. Similar as the MEMS microfabrication technique, which derived from the IC fabrication technology, MEMS packaging technique is also developed from the IC packaging technique but has stricter requirement. Flip chip packaging gradually became the mainstream technology in the development of MEMS device because it is consistent with the characteristics of MEMS device, for example miniaturization, effectiveness, and low cost. Corresponding to the usage of underfiller to reduce residual stress in IC

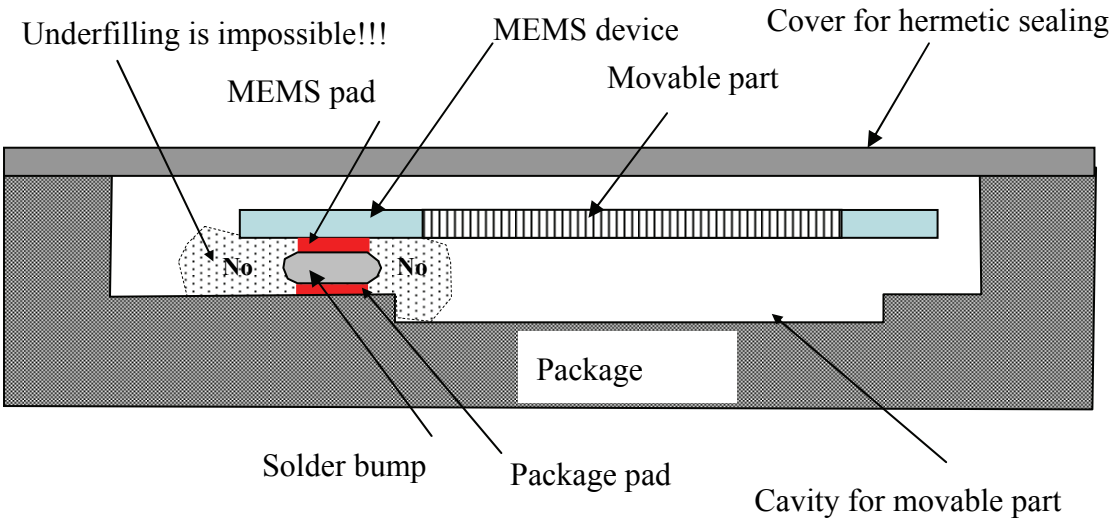

Fig. 5.2. Cross section of flip chip bonding for MEMS device

flip chip packaging, it can not be used for packaging MEMS. It is because MEMS usually has a moving part, which may be filled or contaminated by the underfill material especially in the case of bulk etched device in wafer-thick. Corresponding to the IC flip chip mount cross section (Fig.5.1), Fig. 5.2 gives the MEMS device flip chip packaging considerations. As shown in Fig. 5.2, for MEMS packaging efforts should be made to substitute the function of underfiller. For example, hermetic encapsulation with inert gas would benefit to anti-oxidation. Selection of excellent mechanical strength solder would give long-term reliability and precise mechanical mount. This study aimed to resolve the residual stress problem without using underfiller. On the other hand, compared to IC, MEMS device generally has few electrical pads. Proposed method is to modify the MEMS device structure by designing the electrical pads on spring beams and leaving one pad for ensuring the bonding mechanical property.

5.1.3. Design of stress free sensor structure

Combining with the actual application on a MEMS tilt sensor, the designing architecture is described as follow. The detailed information about the capacitive tilt sensor has been reported in our previous publications [2-3], which demonstrated the high detection resolution at 0.0001 degree class. For easy understanding of the context, the differential capacitive tilt sensor is simply introduced as follow. The sensors were fabricated by anisotropic etching the quartz wafer. The basic sensor structure is depicted in Fig. 1.2. The sensor is composed of sensitive cantilever beam, proof mass and comb electrodes. The excellent electrical isolation property of quartz enables us create comb electrodes in full wafer-thick, which promises large initial capacitance. Compared with Si-based MEMS device, it is no need to consider the isolation concern. Improved sensor structure is given in Fig. 5.3, wherein two spring beams are specially designed for introducing the left side electrode pad and right side electrode pad [4]. When flip chip packaged, the residual stress is expected to be absorbed through the defection of spring beams.

5.2. Experimental

5.2.1. Fabrication of designed tilt sensor

Except for the added two spring beams, the designed sensor has the same basic structure with previous version. The used quartz wafer was 100 μm thick. Anisotropic wet etching technique for getting high aspect ratio gap between movable electrodes and static electrodes was introduced in [5]. The detailed fabrication process, which should pattern the surface wiring and pads and leave metal films on the comb electrode side walls, is described in [3, 6]. Although two spring beams are inserted, no additional treatment is needed because spring beams including leading wiring can be created along with the comb electrodes. In one word, proposed design would not increase the process cost.

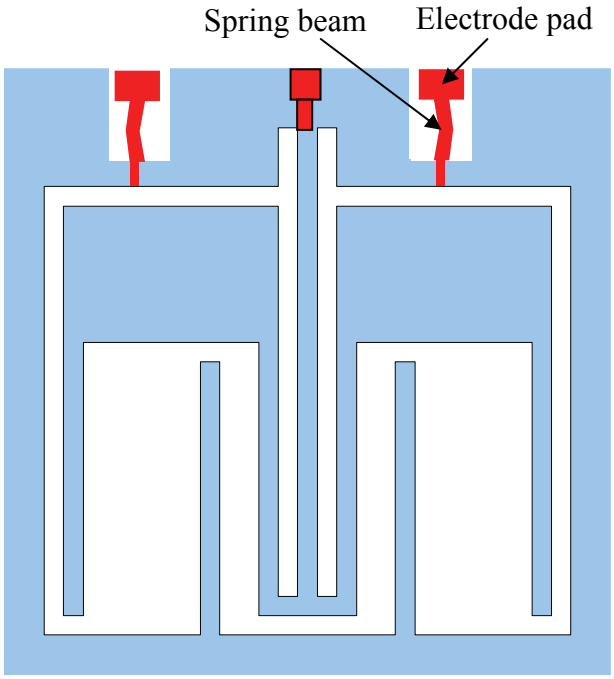

Fig. 5.3. Schematic diagram of proposed design for tilt sensor

5.2.2. Flip chip packaging

A special ceramic package (Kyocera Co., Japan) with a 100 μm deep cavity for movable part was designed for bonding the capacitive sensor. Two kinds of AuSn alloys were used as solder material in this study. These are Au80Sn20 and Au20Sn80, having melting point of 278 ^{o}C and 217 ^{o}C, respectively. The package pads were plated with gold for reliable bonding. The packaging flow is as follow: (1) Forming solder bump on the package pads using AuSn preform film (300μm × 300μm × 100μm, Tanaka Kikinzoku group) through reflowing in nitrogen environment at the peak temperature of 320 ^{o}C for Au80Sn20 and 240 ^{o}C for Au20Sn80, respectively; (2) Arranging and aligning the sensor pads to package pads. (3) Reflowing at the peak temperature of 320 ^{o}C in nitrogen environment. The CTE of the quartz wafer and ceramic are 14 ppm/K and 7.1 ppm/K, respectively.

Sparkle Flux WF-6400 (Senju Metal Industry Co.,ltd.), which is water soluble, was used for forming solder bump and bonding sensor. Detailed bump formation process is as follow: (1) Coating flux on the ceramic package pads; (2) Putting AuSn preform on the pads; (3) Reflowing at 320 ^{o}C for Au80Sn20 and 240 ^{o}C for Au20Sn80, respectively; (4) Washing the bump for removing flux. This is because after reflow treatment, the flux would lose its activity and the flux on the bump surface would hinder the following sensor bonding. The AuSn bumps were washed in pure water at 60 ^{o}C and or in Piraha solution as introduced in Chapter 2.

5.2.3. Evaluation

Thermal cycling was applied on the packaged sensor with and without spring beam structure. The temperature profile is shown in Fig. 5.4. and it specifies the temperature range of -20 ^{o}C (T_{min}) to +120 ^{o}C (T_{max}). The holding time was 5 min and the temperature ramp was not specially controlled.

5.3. Results

5.3.1. Fabricated sensors

Fig. 5.5 shows the fabricated tilt sensors. Fig. 5.5 (a) is the previous design without spring beam and Fig. 5.5 (b) is the proposed sensor design with spring beams. The electrodes and pads were Cr/Au metal films. Here Cr was used as adhesive layer for the well known fact that Au has a bad adhesion with quartz but low electrical resist and

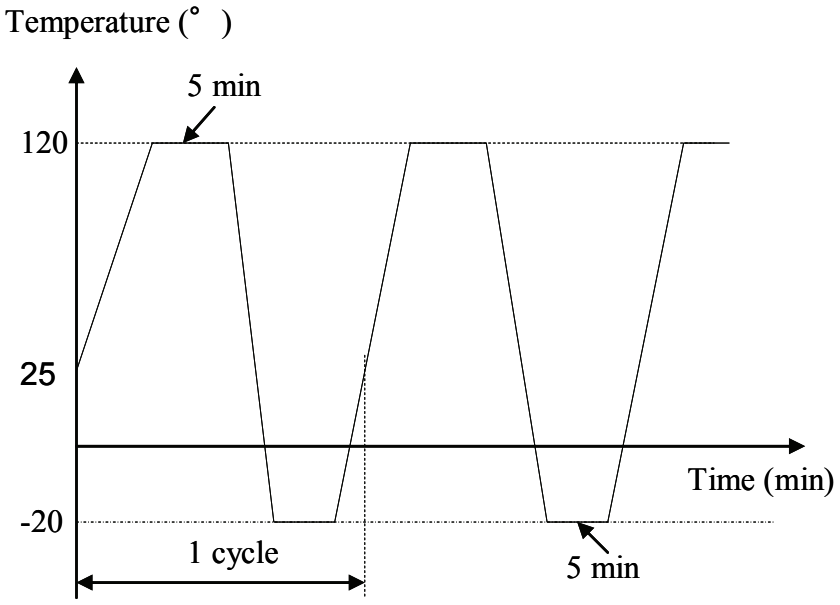

Fig. 5.4. Evaluation of temperature cycles

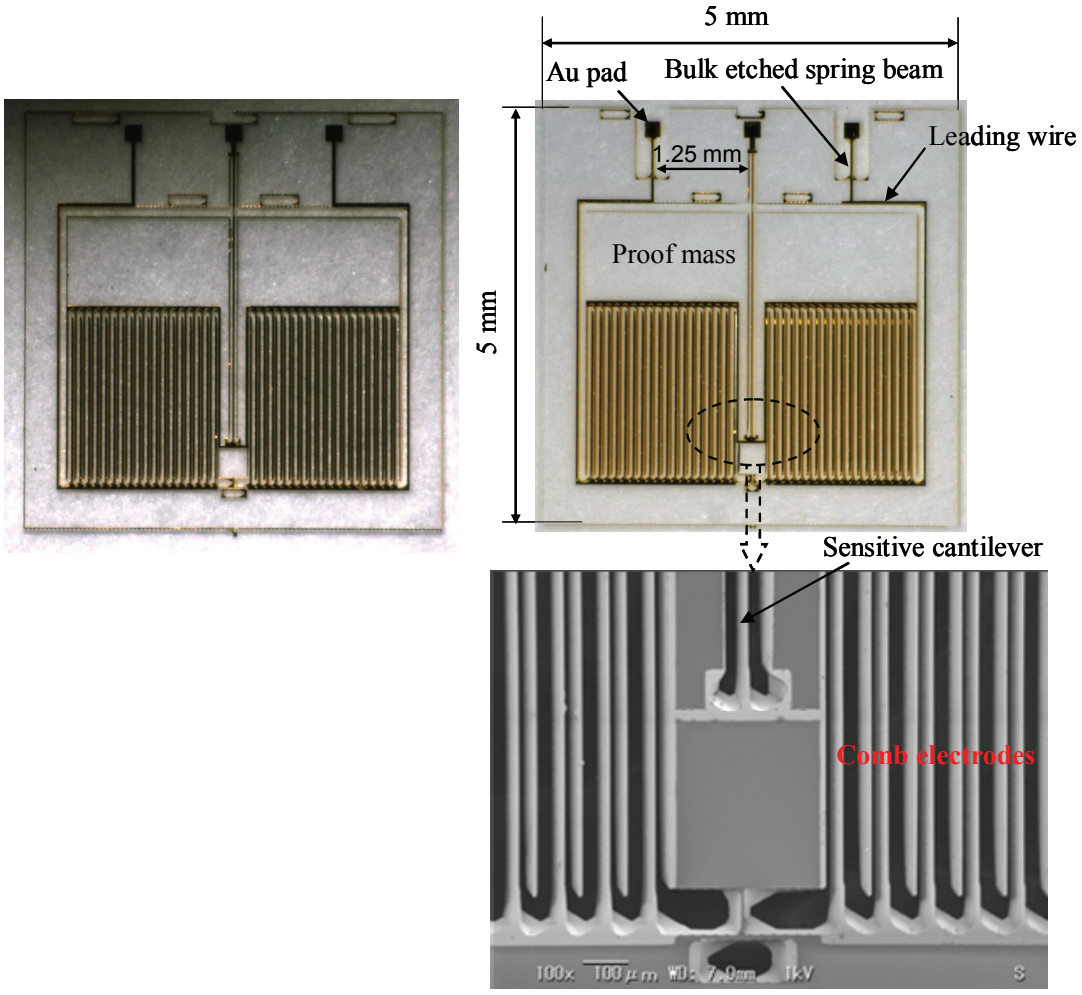

Fig. 5.5. Fabricated tilt sensors: (a) Previous design without spring beam for bonding; (b) Proposed design with spring beams for bonding

good bonding property. The spring beam was 50 μm wide and 500 μm long. The small holes near the spring beams are designed for electrically isolating the electrodes. This is because side wall metal films are continuous. By removing the surface metal films and breaking the through-hole's side, electrical isolation can be achieved.

5.3.2. Packaged sensor

Fig. 5.6 shows the formed bumps. After washing the bumps using pure water, there

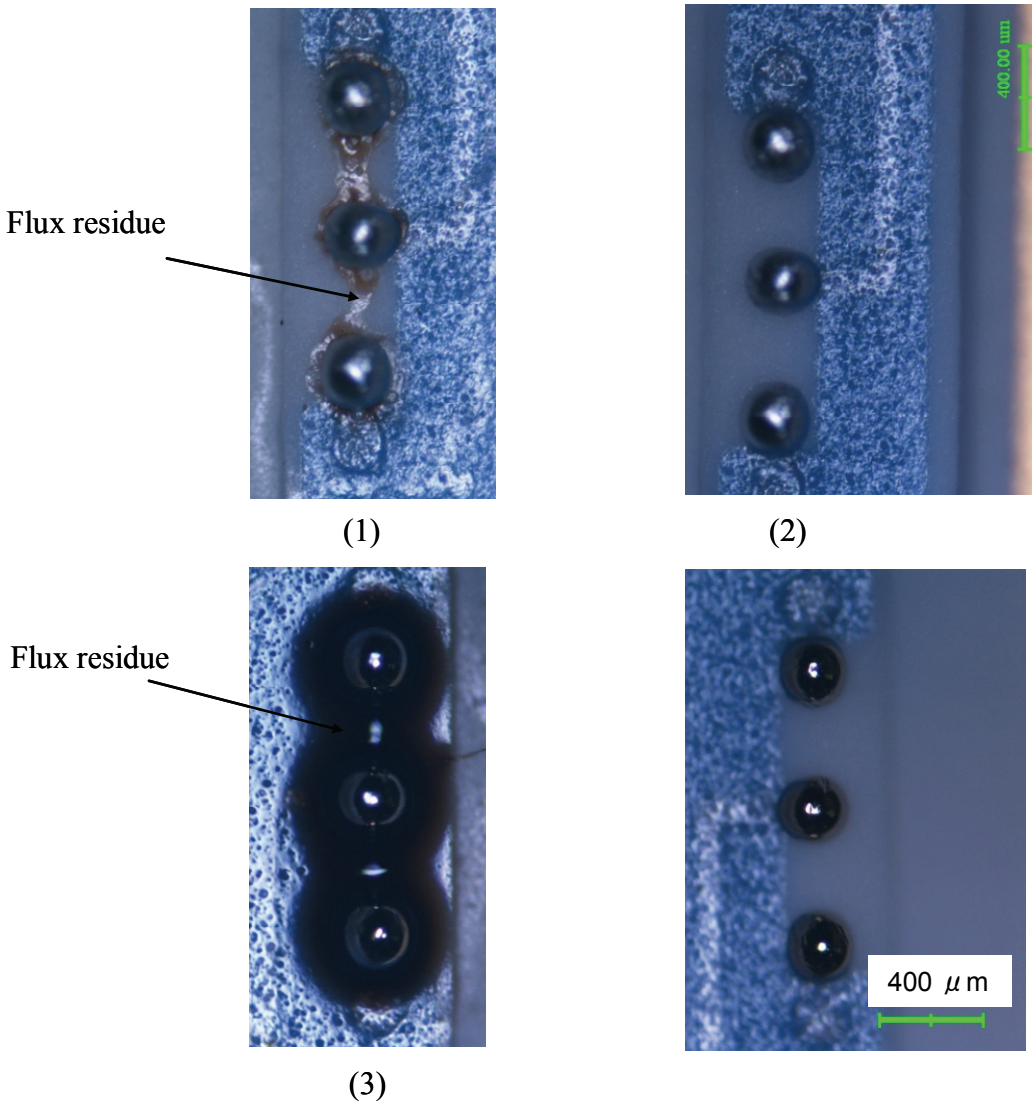

Fig. 5.6. Formed bumps: (1) Au20Sn80 washed with water; (2) Au20Sn80 washed with Piraha solution; (3) Au80Sn20 washed with water; (4) Au80Sn20 washed with Piraha solution

are little residue on the bump Au20Sn, but there are much on the bump Au80Sn20. This is caused by the high reflow temperature. However, washing using Piraha solution can

remove the residues clearly both the Au20Sn80 bump and Au80Sn20. So, in this study for the bonding of sensor, the Piraha solution washed bumps were used. Fig. 5.7 shows the flip chip packaged sensor with spring beams using Au80Sn20 bumps. The solder joint was confirmed using microscope followed by examination of electrical connection using impedance analyzer.

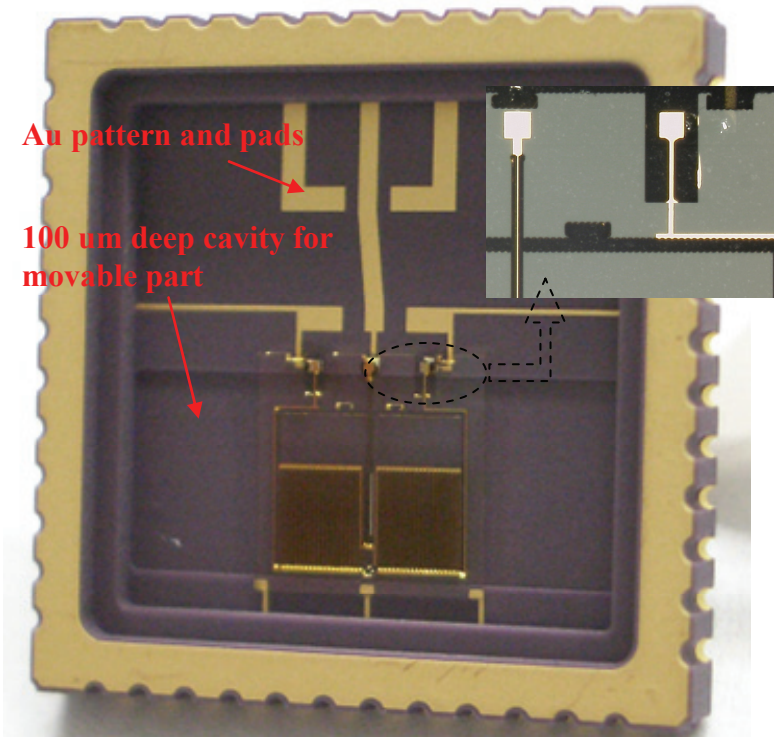

Fig. 5.7. Packaged tilt sensor with spring beam for absorbing residual stress

5.3.3. Thermal evaluation result

After 5 cycles of thermal test as Fig. 5.4, crack was found on the sensor without spring beam (Fig. 5.8) but not on the sensor with spring beam. This result demonstrated the effectiveness of the spring beam. In fact, for the design without spring beam even no

crack occurs, the warpage of the quartz wafer caused by residual stress still influences the performance of the sensor. And the warpage is dependent on the actual environmental temperature, which would change the gap between movable electrode and static electrode.

Further evaluations for the solder joint such as vibration and shock tests are under investigation.

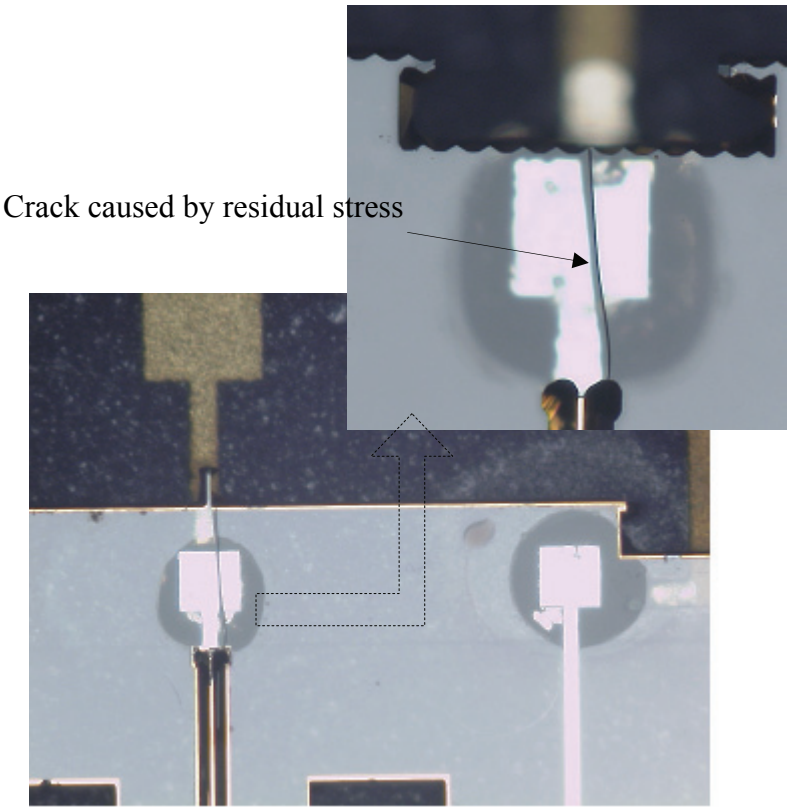

Fig. 5.8. Failure example of the design without spring

5.4. Discussions

5.4.1. Concerns for selection of solder material

Among a relatively large number of Pb-free solder alloys, in this study the Au80Sn20 alloy was selected as the solder material for its high-temperature performance, superior resistance to corrosion, high electrical and mechanical strength [7]. Compared to the low melting temperature Sn-rich alloys, such as Au20Sn80, Au80Sn20 alloy at thermal equilibrium is a mixture of Au_5Sn and AuSn compounds. Thus, there are no tin atoms that are not incorporated in the intermetallic compounds in the eutectic alloy to get oxidized [8]. In the case of IC packaging, solder joint could be protected by underfiller. Otherwise, as discussed above, underfiller could not be used in MEMS devices. This requires the formed solder joint should be self protected from oxidation. Further, the high melting temperature would also contribute to the post-processing steps, such as subsequent capacitance detection IC bonding and package sealing process.

5.4.2. Fluxless requirement

From IC packaging to MEMS packaging, another technique point is the prohibition of using flux, which is necessary to remove oxides on the molten solder and on the base metal, and to shield the contact solder surface from further oxidation. For the MEMS devices, it might be very difficult to completely remove flux residues that result from the use of fluxes. The fluxes trapped in the gap can degrade the performance of the device and may also cause long term reliability problems [9-10]. Proposed design also contributes to the self alignment during reflow, because large distance between pads is admitted.

5.5. Summary

A new design for solving the residual stress problem in MEMS flip chip packaging was proposed. Based on this idea, the dependence on solder melting point is reduced. To our knowledge, it is the first report concerning residual stress in MEMS packaging.

Proposed design was applied on the quartz MEMS based capacitive tilt sensor, thermal cycling tests demonstrated the effectiveness. Proposed method is expected to apply on other MEMS device packaging.

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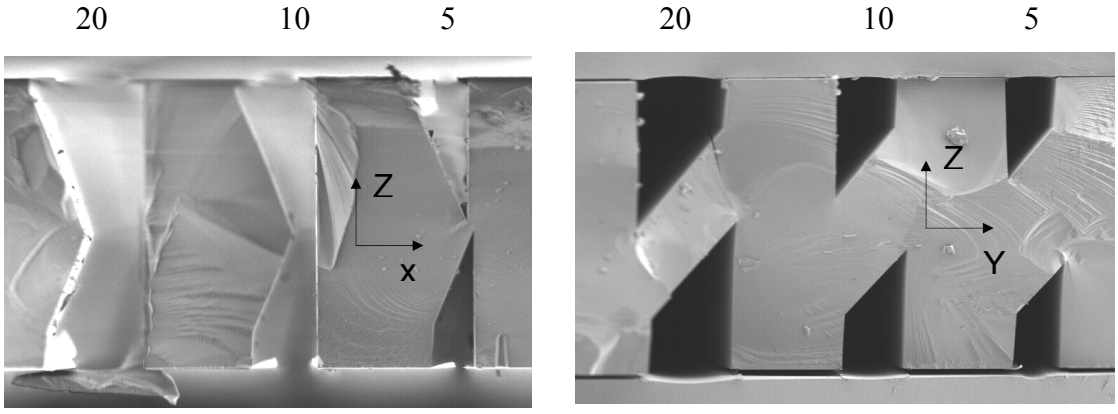
Chapter 6 Fabrication of two-axis tilt sensor

6.1. Introduction

Although most micromachining is focused on Si, quartz exhibits great interest for its piezoelectric property, optical and electrical properties, which compensate the commonly used MEMS material Si. One essential reason for the lack of interest in quartz is that the amount of knowledge and manufacturing equipment for quartz is neither as extensive, nor as widespread, as for semiconducting materials such as Si and GaAs [1-2]. The drawback of quartz as MEMS material is that the electronic circuit associated with the device is not realized on the same chip. This one-chip conception is clearly an exclusive property of silicon at the moment, but for many applications, it may not be really necessary and gives rise to very tricky compatibility problems [3]. System in one package (SIP) technique gives more opportunities to non-Si MEMS materials.

Recently, MEMS-based tilt sensor draws great attention for the relatively low cost



(a) X direction (b) Y direction

Fig. 6.1 Cross-section of double-sided etched quartz profiles with initial widths of 5, 10, 20 μm from right to left on 100 μm thick z cut quartz wafer; (a) Etched at x direction for 1 hour; (b) Etched at Y direction for 1.5 hours.

to performance [4-5]. However the reported detection resolution (0.5 degree) is too low to act as level detector, which is widely used in semiconductor manufacture equipment adjustment with a high resolution of 0.0001 degree class. On the other hand, existing high resolution tilt sensor suffers from the big size, which usually has a dimension of several tens mm in length, width and height. This research aims to develop such a highly sensitive tilt sensor. A single axis capacitive tilt sensor has been developed by bulk micromaching of quartz wafer, which was presented earlier [6]. Generally, the sensing element is composed of sensitive cantilever, mass proof and comb electrodes. Concerns about the design and optimization of the sensor which utilizes the X axis (quartz crystal axis) direction side wall, should be referred to our previous publication [6].

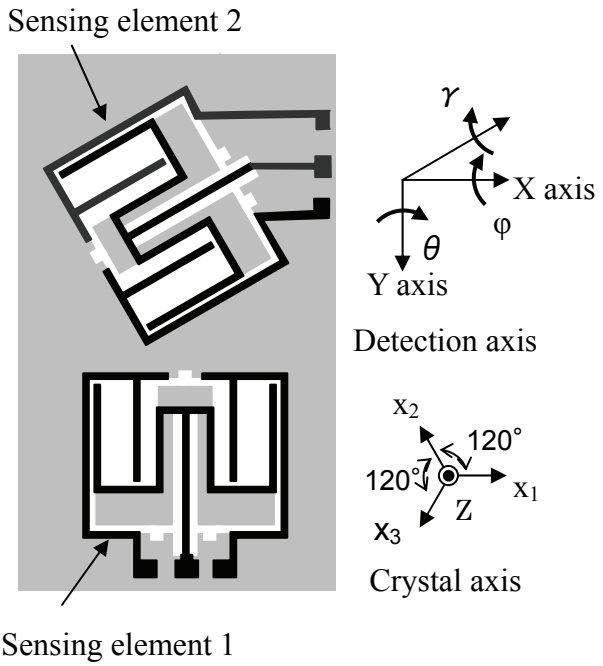


Fig. 6.2 Schematic diagram of two-axis tilt sensor

A number of recently developed applications require the adoption of dual-axis tilt sensors. Using two single axis tilt sensors is a simple way, however it means high-cost

and it is also difficult to precisely align the angle between the two sensors. In this research, a new design of two-axis sensor is proposed with two sensing elements on one chip. Ideally to fabricate two-axis tilt sensor, sensing element 2 would be polarized 90° to sensing element 1. Unfortunately Y axis (quartz crystal axis) direction side wall can not be used for comb electrodes due to the complex side wall shape and low etching rate. Fig. 6.1 shows the double-sided etching results at X direction which was used for fabricating single axis tilt sensor and Y direction in saturated ammonium bifluoride solution at 87 ^{o}C. In the X direction, the quartz wafer was etched through in one hour at the space of 10 μm, however in the Y direction it can not be done even in 1.5 hours at the space of 20 μm. Proposed two-axis tilt sensor integrated two same sensing elements on one chip at an interval of 120° (Fig. 6.2) utilizing the threefold symmetry property of quartz. Sensing element 1 detects the tilt angle around Y axis (detection axis) giving the output θ and sensing element 2 detects the information of Y axis (θ) (detection axis) and X axis (φ) (detection axis) giving output γ. The tilt angle around axis X (φ) is given by the following formula (1).

$$\varphi = (\gamma + \theta \cdot \sin 30°)/\cos 30° \quad \text{.....(1)}$$

6.2. Fabrication and packaging method

6.2.1. Fabrication process

For fabricating the MEMS sensor, several microfabrication techniques should be involved including anisotropic etching technique [7], 3-D patterning technique, and metal deposition technique for high aspect ratio microstructure. An improved lift off process [8] was developed for patterning the surface leading wire, pads but leaving metal film on the electrode side wall. In this process, no resist coating is needed for the high aspect ratio electrode gap side wall.

Fabrication process has been introduced as Fig. 3.10. in Chapter 3.

6.2.2. Side wall metal deposition

In this study, metal films should be deposited on the side wall of comb electrodes for forming capacitance. Generally, higher aspect ratio, worse step coverage. Several methods have been reported for improving step coverage, such as long-throw low-pressure sputtering technique, collimator-based directional deposition technique [9-12], and oblique angle physical vapor deposition [13]. In this research, for getting good step coverage on the side wall of the high aspect ratio gap between movable electrodes and static electrodes, wafer rotation sputtering system, which is considered to have the advantages of methods mentioned above, was adopted. These are the long distance of 150 mm between target and wafer holder and all oblique angles facing the

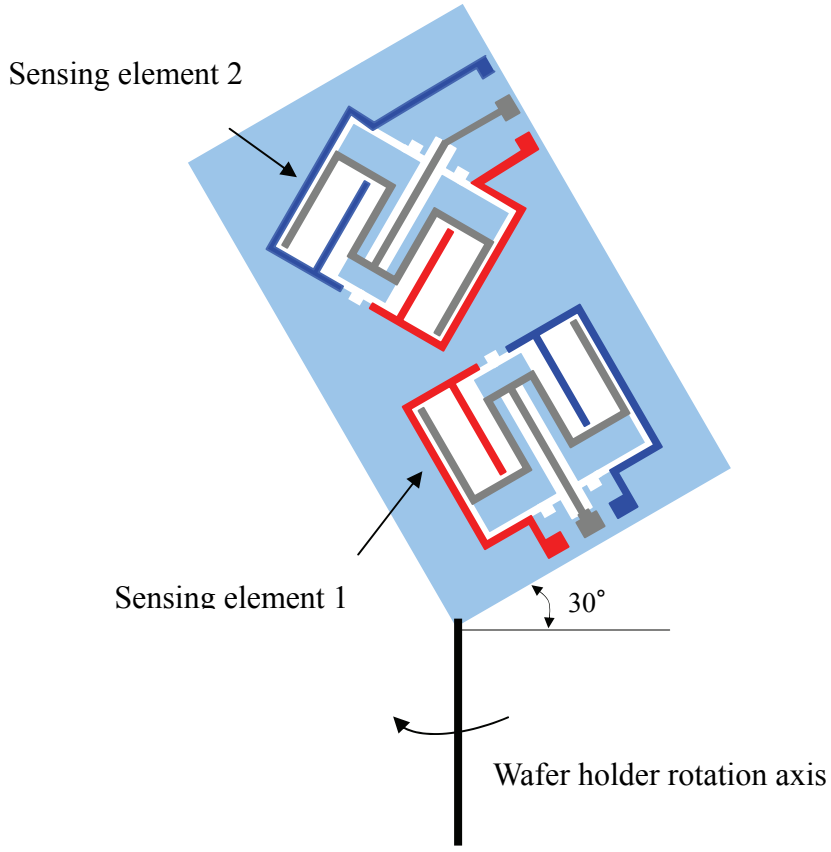


Fig. 6.3. Wafer set up for getting same side wall metal deposition on two sensing elements

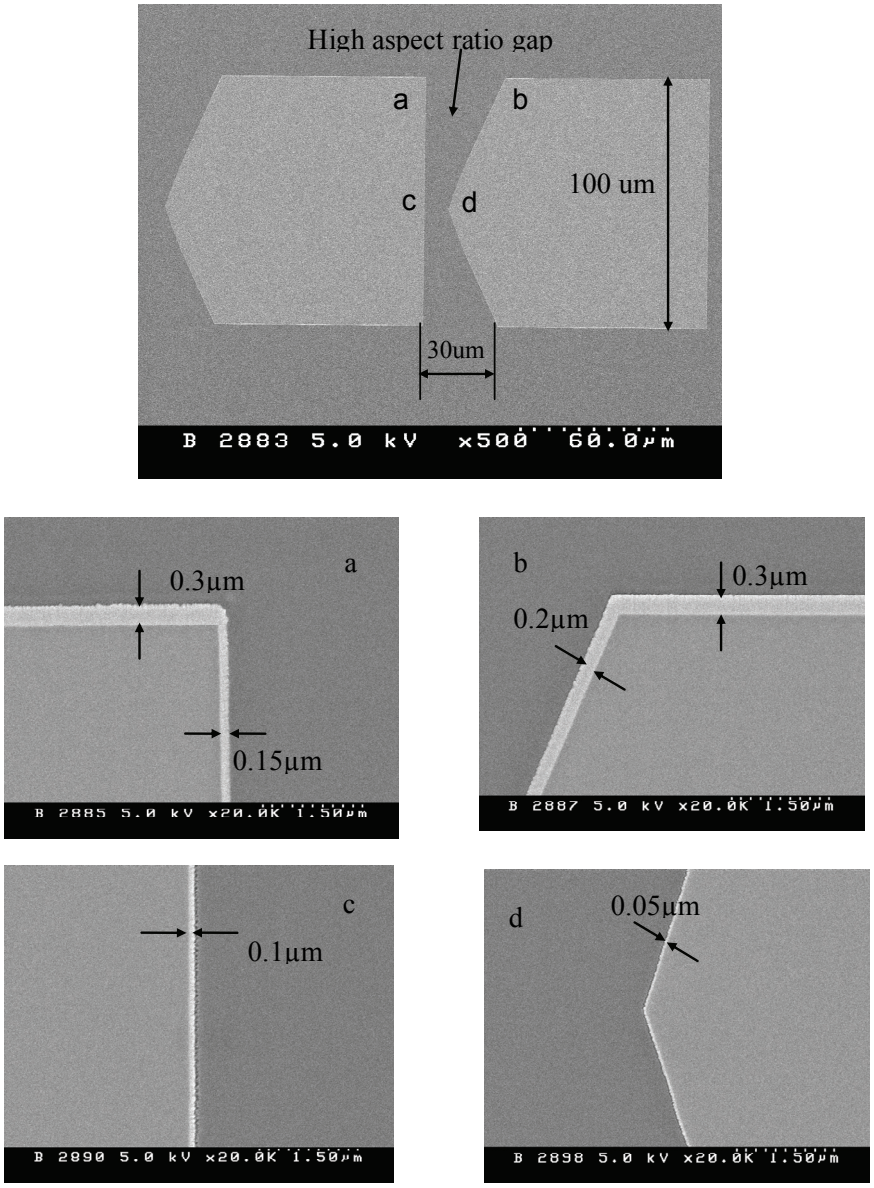


Fig. 6.4. SEM pictures of the high aspect ratio gap and observed step coverage

target.

For achieving the same step coverage on the two sensing elements, the quartz wafer was polarized 30° to the wafer holder rotation axis which ensured all the comb electrodes polarized at the same angle (Fig. 6.3). Examination experiments were made

by investigating the step coverage of the same gap as the comb electrodes by sputtering 300 nm Cr film on the surface. The working pressure was set below 2 mTorr. The result is shown in Fig. 4 Minimum 50 nm thick film was observed at the center of the tapered side wall. This result suggests that for getting minimum 100 nm thick metal film on the side wall, 500~600 nm should be deposited on the surface.

6.2.3. Flip chip packaging

Flip chip technology has been widely accepted as a means for maximum miniaturization with additional advantages, such as shortest interconnect length for minimum signal disturbance and simultaneous interconnection leading to reduced process times. A ceramic package was designed for flip chip mounting the MEMS sensor as Fig. 6.5. The packaging process is as follow: (1) Creating AuSn bump on the ceramic package pads using 100 μm Au20Sn80 film by reflowing at 240 ^{o}C; (2) Setting the sensor and aligning the sensor pads to package pads; (3) Reflowing in nitrogen environment at the peak temperature of 240 ^{o}C for 30 s.

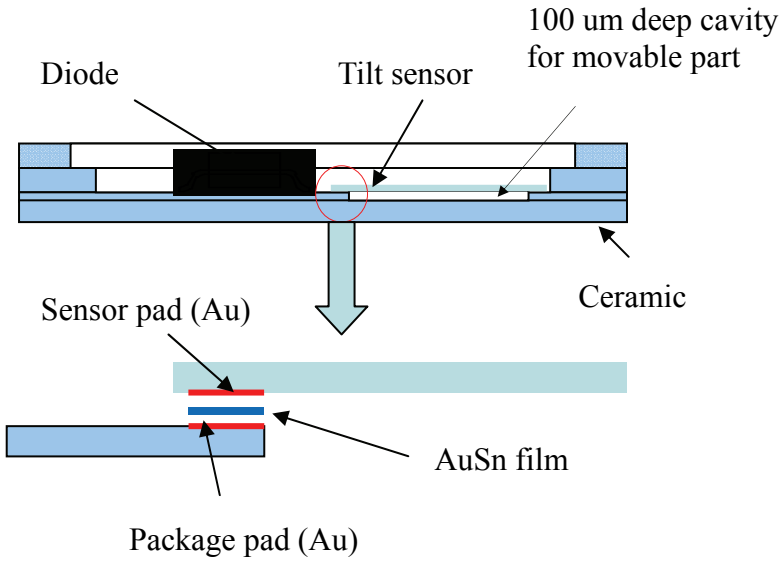


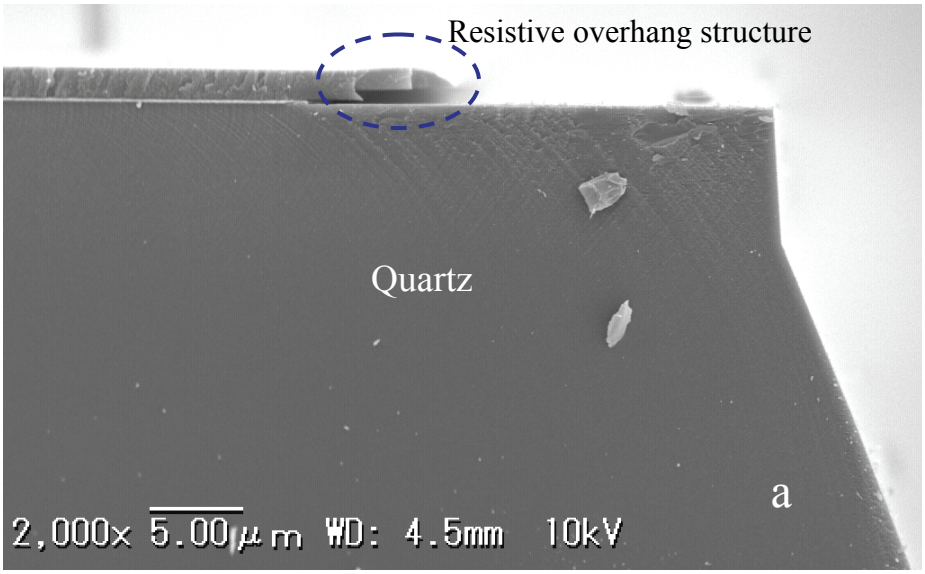
Fig. 6.5. Schematic diagram of flip chip packaging

6.3. Result and discussions

6.3.1. Fabricated tilt sensor

The key feature of the process is to create a high aspect ratio undercut to reduce the step coverage on resist overhang. Further, the overhang structure should be hard enough to resist the aggressive quartz etchant. A bi-layer (top image resist Shipley S1808 and bottom lift off resist LOL2000) lift-off process was adopted. The high aspect ratio hard undercut was created using a two-step development method and the detailed information should be referred to previous presentation [6]. Fig. 6.6 demonstrated that the overhang can withstand the aggressive substrate etchant and separate the metal films under and on resist: (a) after quartz etching; (b) after sputtering Cr/Au/Cr metal films.

Fabricated two-axis tilt sensor is shown in Fig. 6.7. Fig. 6.7 (a) shows the top view of the full sensor with clearly patterned leading wire and pads. Fig. 6.7 (b) demonstrated the successful quartz etching for comb electrodes. Fig. 6.7 (c) shows the



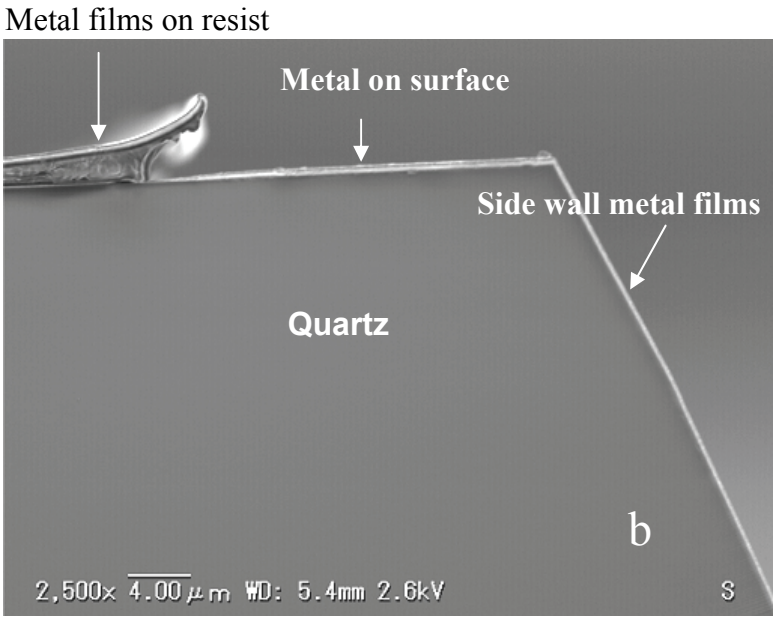


Fig. 6.6. Cross section of the overhang structures: (a) after quartz etching; (b) after sputtering metal films

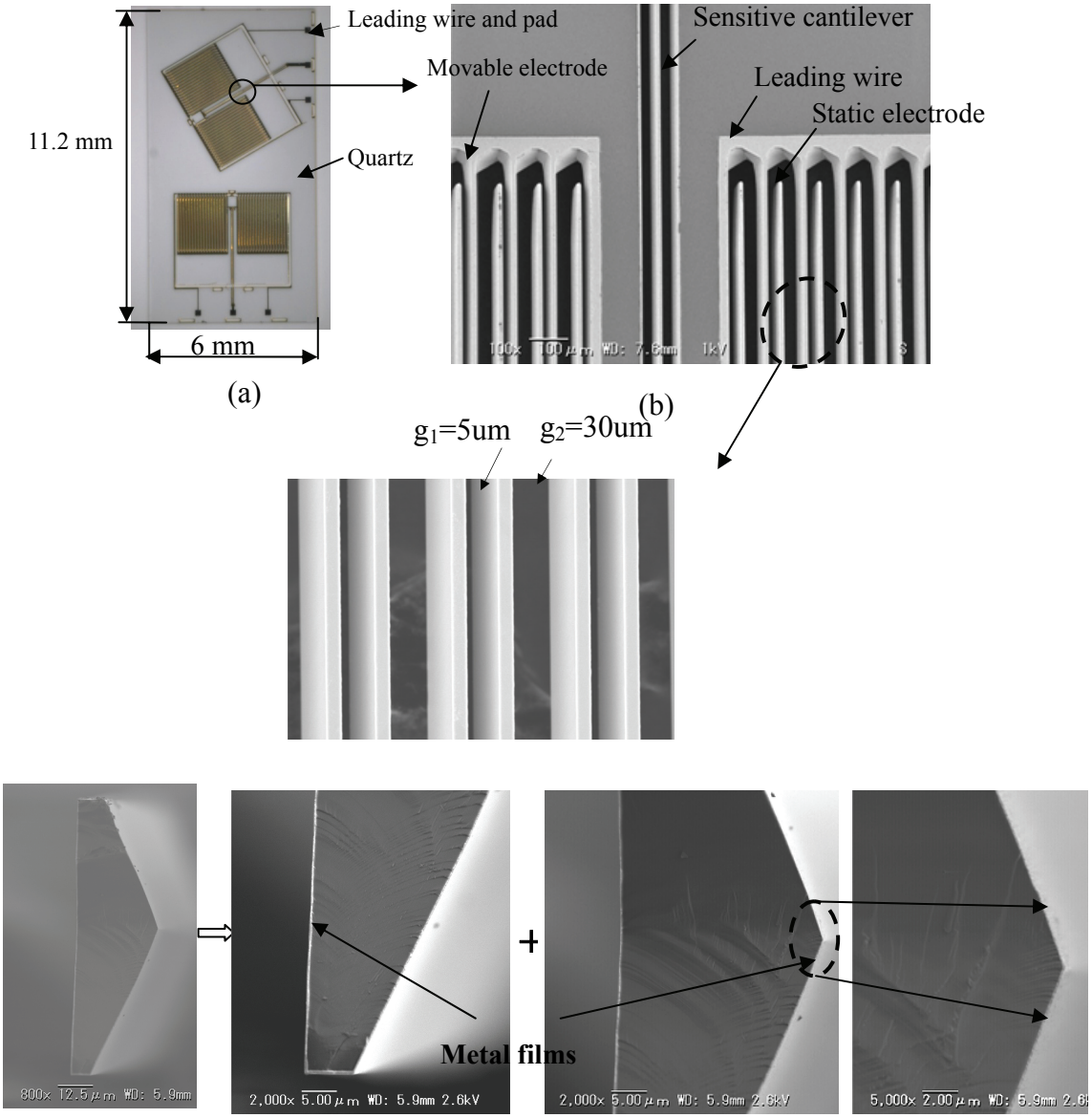


Fig. 6.7. Fabricated two-axis sensor: (a) Optical picture of the full sensor; (b) SEM pictures of sensing element; (c) Cross section of the electrode and magnified pictures for confirming the side wall metal films.

cross section of the electrode. The side wall metal films can be examined by the magnified pictures. This result demonstrated the success of the improved lift off process which patterned the surface metal films and protected the side wall metal films. The good step coverage caused by proposed rotation sputtering system was also confirmed.

6.3.2. Flip chip packaged sensor

In the last 10 years, lead-free materials became the mainstream for electronic bonding. Among them, AuSn is a commonly used alloy especially for high frequency operation. At first, AuSn bump was formed on the ceramic package via reflow treatment at 240 ^{o}C (Fig. 6.8). Then the sensor was set on the package and aligned pads to pads. Mounting was formed at 240 ^{o}C (see Fig. 6.9). Unfortunately crack was observed after reflow process. It is caused by the residual stress which generated in the process of reflow due to the big difference of thermal expansion coefficient between ceramic (5.5 ppm/k) and Z cut quartz (14 ppm/k) as well as the long distance (9 mm) between the two sensing elements pads. Solution was made by inserting spring structure between the two sensing elements for absorbing the residual stress. The improved structure is shown in Fig. 6.10(a). Fig. 6.10(b) shows the successful mounting result and the deflection of

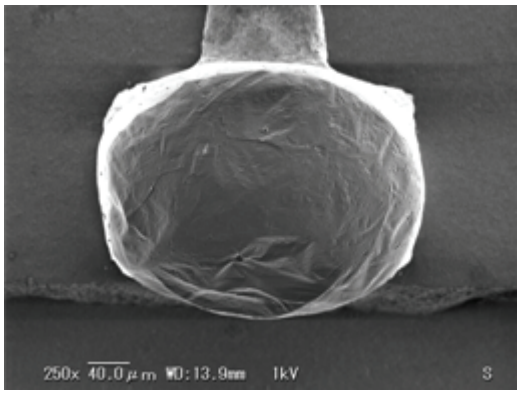


Fig. 6.8. SEM picture of formed AuSn bump

the spring can also be observed clearly. And the measured deflection of 18 μm agreed well with the calculated value of 15.1 μm, wherein the melting point of AuSn is 217 ^{o}C. This demonstrated our solution for reducing thermal stress in the case of long distance pads is simple and effective, especially in MEMS packaging where underfill can not be used.

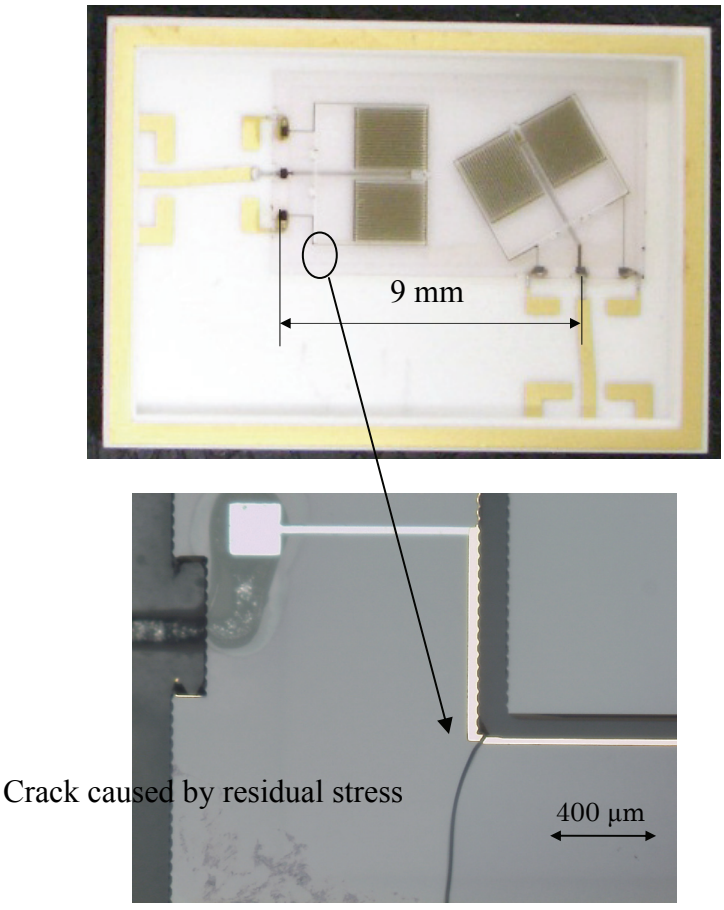
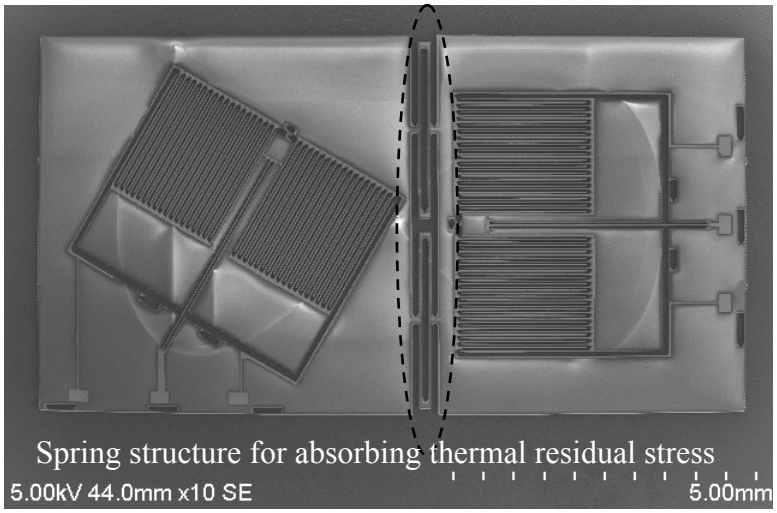
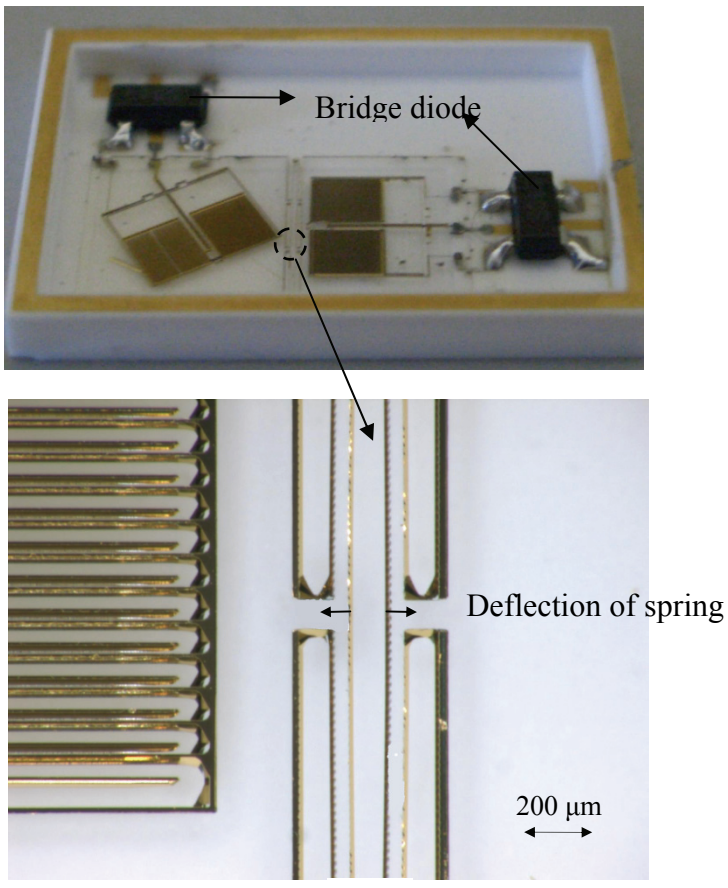


Fig. 6.9. Failure example of flip chip mounting



(a)



(b)

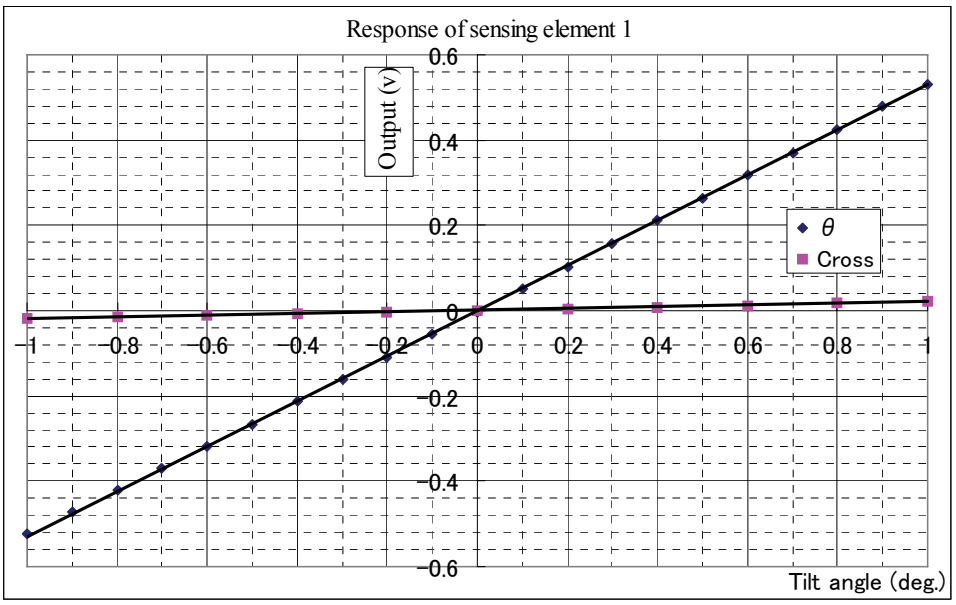
Fig. 6.10. Successful packaging by inserting spring structure for absorbing the thermal residual stress: (a) SEM picture of improved sensor structure; (b) Packaged tilt sensor

6.3.3. Sensitivity evaluation

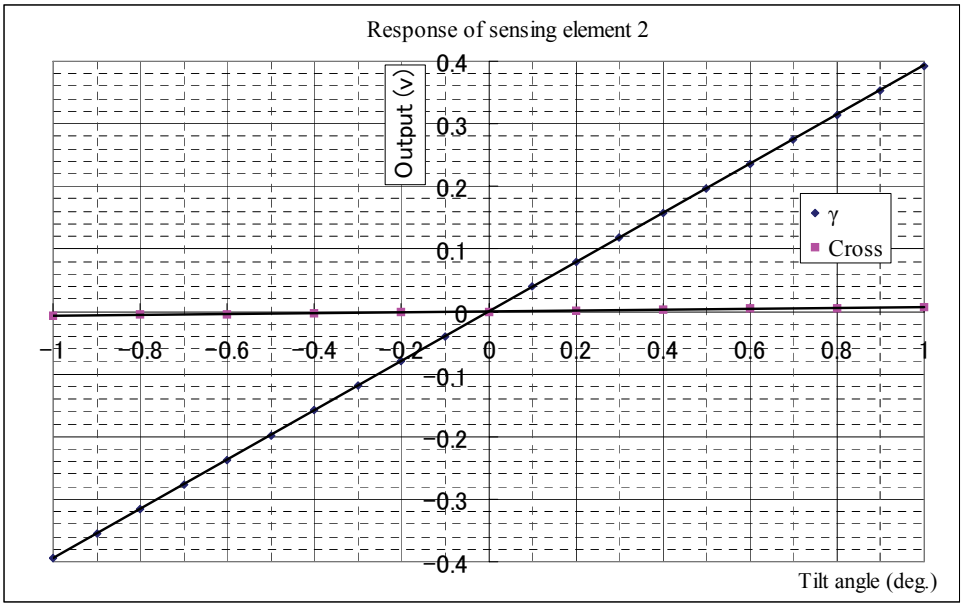
Fabricated tilt sensor was evaluated using bridge diode based capacitance detection circuit, which has been presented previously [14]. Measurement was performed in the range of ±1° at room temperature. Evaluation was performed on a specially designed measurement machine, which is 1 m long and has a high tilt angle resolution of 0.0001° at room temperature. Applied voltage was 5 V at 1 MHz. Fig. 11 shows the examination results with good linearity of sensing element 1 (a) and 2 (b), respectively. The sensitivity was confirmed to be 529 mV/° for sensing element 1 and 394 mV/° for sensing element 2, respectively (Fig. 6.11). And the cross sensitivity was 19 mv/° and 7 mV/° for sensing element 1 and 2 respectively. Both sensing elements showed high resolution for 0.001° level detection. Fig. 6.12 shows an example data of accuracy measurement at 0.001° of sensing element 2.

The output difference between the sensing element 1 and sensing element 2 is considered to be the misalignment of double-sided (upper and lower mask alignment) patterning. Fig. 6.13 gives an example picture of misaligned electrode structure. Because the comb electrodes of sensing element 1 and 2 are not parallel, any alignment error will give different effect to sensing element 1 and 2, which produces different gap between the comb electrodes and width of cantilever resulting in different detection sensitivity.

Current work is focusing on evaluating the detailed characteristic, such as temperature dependence, damping effect et al.



(a)



(b)

Fig. 6.11. Sensor response Vs tilt angle: (a) Sensing element 1; (b) Sensing element 2.

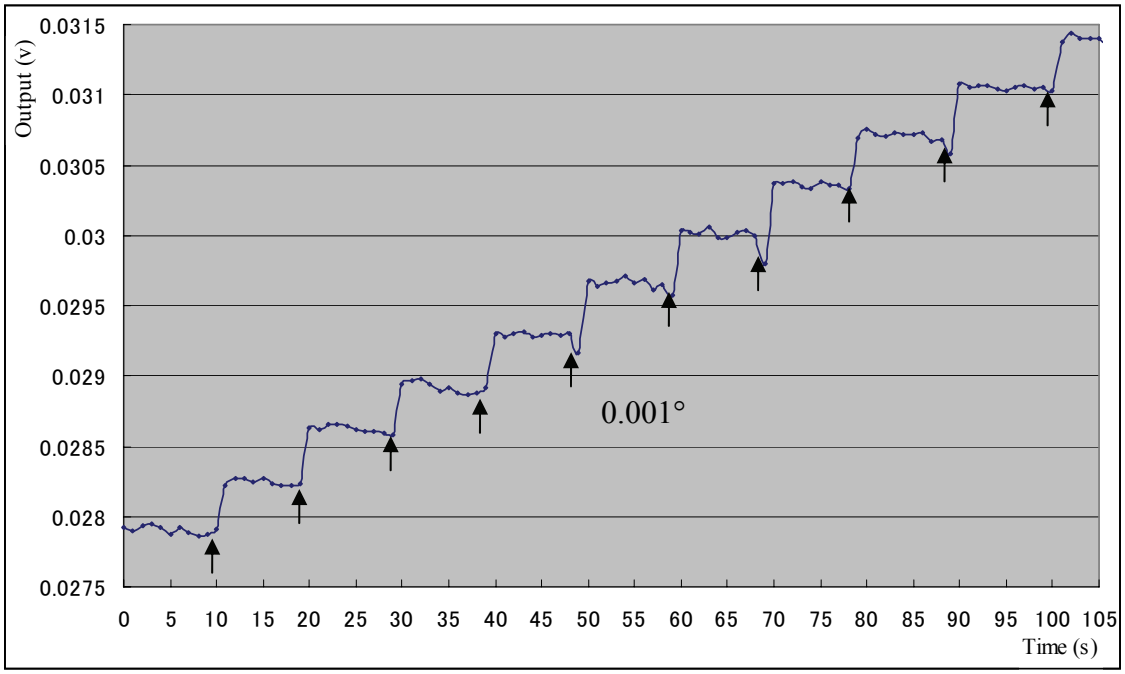


Fig. 6.12. An example data for high precision measurement at 0.001° on sensing element 2.

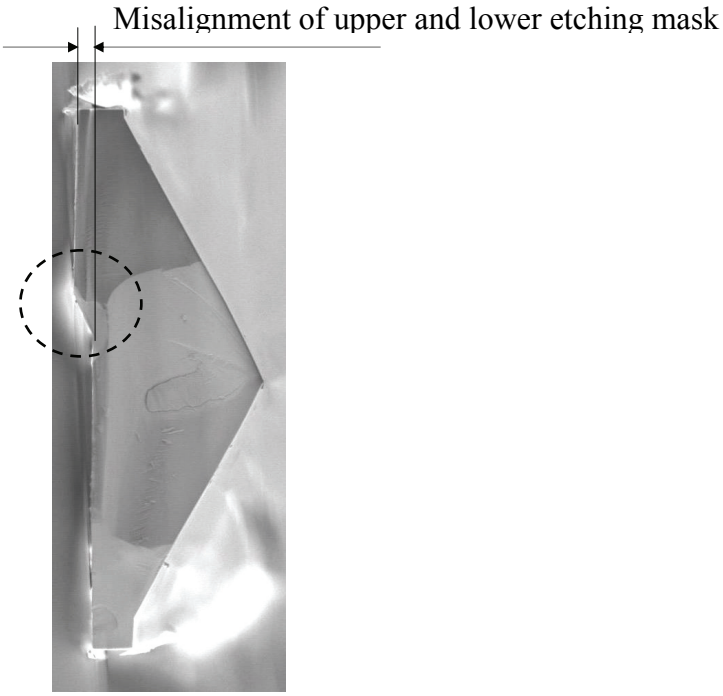


Fig. 6.13. Cross section of misaligned electrode

6.4. Summary

A new highly sensitive two-axis capacitive tilt sensor was developed based on bulk micrmachining quartz techniques. Two same sensing elements are designed on one chip for two-axis detection utilizing the threefold symmetry property of quartz wafer. Several microfabrication techniques and packaging technique were developed. These are anisotropic quartz etching technique, 3-D patterning lift off process and wafer rotation sputtering system for improving step coverage. A spring structure was designed for stress-free flip chip packaging. Fabricated tilt sensor was evaluated using a bridge-diode based capacitance detection circuit. Both sensing elements showed high sensitivity with 529 mV/° for sensing element 1 and 394 mV/° for sensing element 2, respectively. And high accuracy detection of 0.001° was examined on the two sensing elements. To our knowledge, it is the first report for 0.001° level tilt angle detection on the small size chip of 11.2 mm×6 mm×0.1mm.

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Chapter 7 Conclusions

Most MEMS interests are focused on silicon, because MEMS fabrication techniques mainly derived from integrated circuit (IC) fabrication, especially the element separation technique of power electronics and the great amount of knowledge has been accumulated to date. However, the concept of MEMS is not restricted to this material and other materials can be interesting for realization of specific devices. Quartz is such a material. As a MEMS material, quartz exhibits interesting properties that complement silicon. These include electrical insulation, piezoelectricity, UV-transparence, low thermal conductivity, chemical inertness and so on.

This research reports microfabrication technologies for fabricating a capacitive tilt sensor and the realization of two-axis tilt sensor using developed technologies.

Chapter 1 is introduction section. In this section, a brief introduction of the concept, attraction and history of MEMS is first given. Subsequently, the value and importance of some quartz properties and their potential applications to MEMS devices are also indicated. Targeting on realizing a capacitive tilt sensor, the basic quartz MEMS fabrication process and necessary improvements are emphasized. These are anisotropic wet etching technology, 3-D patterning technology, metal step coverage deposition technology, MEMS flip chip packaging technology.

Chapter 2 presents bulk wet etching technology, especially anisotropic etching technique for high aspect ratio microstructures. The precise 3-D microstructures with a high aspect ratio are needed in many MEMS devices. Z cut quartz wafer is usually used in MEMS device because of the high etching rate at Z direction compared to etching rate at directions vertical to Z axis. Experimentally, z cut wafers were etched in saturated ammonium bifluoride solution at 87 degrees C. Mask patterns were designed with initial opening widths of 5, 10, 20, 50, 100 and 200 μm. Large width 200 μm pattern was for observing the whole etching profile and minimum 5 μm was for discussing the possible high aspect ratio microstructure. Because α-quartz is threefold

symmetry, the polar angles of mask patterns was set from 0° to 120° with an interval of 5° at the beginning of +x direction. The side wall profiles were observed using the scanning electron microscopy (SEM) and plotted dependent on the polar direction. This research focused on investigating high aspect ratio trench and through-hole, which were dependent on the polar direction to the crystal axis. Aspect ratio in dependence on polar direction was also plotted and trenches with aspect ratio > 3 could be achieved at polar angles between 30° to 60°. The possibility of application for microcapillary was discussed, and the trench at 45° was considered best.

Double-sided etching technique was used for manufacturing through-hole structures. Through-hole at 0° was demonstrated effective for fabrication of capacitive MEMS tilt sensor. Through-holes at 15° and 105° were proposed for fabrication of 90°-arranged two axis capacitive tilt sensor, taking advantage of the twofold symmetry property around X axis and threefold symmetry property around Z axis. The importance and preparation method of high quality Au/Cr etching mask were also discussed for deep wet etching quartz wafer.

Chapter 3 reports a novel 3-D patterning process. In traditional lithograph process, for patterning 3-D microstructures, photoresist should be coated on the whole wafer including side wall and bottom wall. And in some cases, special exposure equipment is also needed. In reality, it is difficult to be realized especially for high aspect ratio microstructures. Proposed bi-layer (top image resist Shipley S1808 and bottom liftoff resist LOL or LOR) lift-off process does not need to coat resist after etching substrate (forming 3-D microstructure). Resists are coated and patterned with an overhang profile on substrate before it is etched and before the metal film deposition. The key feature of the new lift off process is to create a resist over profile, which should be deep enough to reduce step coverage and durable to aggressive substrate etchant. Two-step development method was developed for achieving such an overhang. The resist profile is optimized by development time in the two-step development process. Using this process, quartz based capacitive tilt sensor, which has a high aspect ratio comb electrode gap, was fabricated. Further, high frequency resonator, which has a big thickness difference

between the supporting part and resonator part, was also fabricated. Fine pattern as 2 um/5 um at line/space was also achieved on the microstructure including 51 um trench at an aspect ratio of 2.7.

Chapter 4 proposes a wafer rotation sputtering system was for improving step coverage on 3-D microstructures. Generally, for 3-D microstructures, higher aspect ratio, worse step coverage. Several methods have been reported for improving step coverage. Directional physical vapor deposition (PVD), such as long-throw low-pressure sputtering technique and collimator-based directional deposition technique, suffers from poor efficiency for the big loss of target atoms. And these techniques were mainly developed for improving the bottom step coverage. Oblique angle physical vapor deposition (OAPVD) technique improves the side wall step coverage by rotating wafer at the tilted angle. However, both long-throw deposition and OAPVD deposition suffer from the asymmetry problem on the wafer edge. Proposed sputtering system by rotating and revolving wafer solves these problems. Test deposition experiment was done on specially fabricated high aspect ratio (3.3) through hole on quartz. Good step coverage on the side wall with a minimum of 0.16 was demonstrated. By optimizing the sputtering conditions, such as working gas pressure, wafer rotation rate and sputtering power, much better step coverage can be expected.

Chapter 5 introduces a stress free MEMS flip chip method. Residual stress caused by the large coefficient of thermal expansion (CTE) mismatch between the device and package is a notorious problem in flip chip bonding. Using an underfilling material to distribute the residual stress and retain the mechanical reliability of the solder joints is a common method for bonding IC and surface micromachined MEMS devices. However, for the bulk etched MEMS device, which is composed of static part and movable part in wafer-thick, underfiller can not be applied because it may flow into the movable elements. Effort was made on improving the MEMS structure. As an example, quartz-based MEMS capacitive tilt sensor, which has three electrical pads should be bonded, was improved by putting the two side pads on spring beams. The torsion beam is designed for absorbing the thermal stress when bonded. Experimentally,

high melting point alloy Au80Sn was selected as the solder bump because it has excellent mechanical strength and hard to be oxidized. Sensors with and without spring beams were flip chip bonded. After thermal cycling tests from -20 ^{o}C to 120 ^{o}C, cracks were found on the samples without spring beams but not on the ones with spring beams. These results should thank to spring beam structure.

Chapter 6 presents a two-axis capacitive tilt sensor on one chip, which is designed and fabricated using the developed technologies. Two same sensing elements with a polar angle of 120° were fabricated using bulk anisotropic wet etching technique on one quartz chip. Sensing element 1 detects the tilt angle around Y axis giving the output θ and sensing element 2 detects the information of Y axis and X axis, giving output γ. Tilt angle φ around X axis can be calculated from θ and γ. The sensor was mounted on a designed ceramic package by flip chip method. A special spring structure was inserted between the two sensing elements for absorbing the residual stress caused by reflow process. The sensitivity of the fabricated sensor was evaluated using diode bridge capacitance detection circuit. In the range of ±1°, voltage outputs are 529 mV/° for sensing element 1 and 394 mV/° for sensing element 2 respectively. The detection accuracy of 0.001° was also examined. To our knowledge, it is the first report, for achieving a sensitive two-axis sensor on one chip with small dimension as 11.2 mm× 6mm×0.1 mm.

In the next step, for the wide application of quartz MEMS, efforts will be done in the following topics. (1) Quartz etching simulator. For precise quartz MEMS design, a quartz etching simulator will be established using the experimental data; (2) High quality Au/Cr metal films. The adhesion strength, residual strength of Au/Cr films are dependent on the sputtering conditions. Optimization of the sputtering parameters will be the next work. (3) Fluxless packaging. Fluxless bonding process is needed for MEMS packaging because fluxless residual would influence the performance of MEMS devices.

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Patents:

1. 植田敏嗣、梁金星：特開 2008-26252 デバイスの製造方法及びこれを用いた傾斜センサ
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